PROTON-SPDAU

400MHz FPGA based Transient recorder

FPGA x3 **1 GByte SDRAM**
Analog In/Out **Digital In/Out**

Applications

Spectroscopy Measurements

Material Characterisation

Hardware in the Loop

Mid Frequency Signal generation

HF digital signal processing

Test Automation

PROTON-SPDAU is a high speed data acquisition system with high storage capacity designed to be used as recorder/processor of wide bandwidth long transient signals.
It integrates an automated averaging engine for multiple measurements up to 300ms long with a sampling frequency of 400MHz.

In the Lab

System resources can be controlled/accessed remotely via ethernet by means of a windows dynamic library **spdaulib.dll** encapsulates all communication routines to program the system from standard software like MATLAB and LabView, or open source scripting environments like OCTAVE and PYTHON.
An embedded operating system provides integrated GUI on a QVGA RGB display

Customer Specific

Flexible and versatile hardware/Software allows the system to be transformed into a custom product with low effort. Application development may be based on a mixture of embedded C , Python scripting and HDL.
C language and PYTHON targeted for embedded Linux running 500MHz ARM processor integrated in PROTON-SPDAU. Prefered HDL targeted for three diferent Xilinx FPGA dynamically programmable via Xilinx Select Map mode.

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*"PROTON-SPDAU is a variant of **PROTONV2-3M07**, a powerful and versatile digital signal processing platform that is a competitive starting point for developing customer specific applications"*

Features

- ❑ 1xADC 14bits@400MHz sampling frequency.
- ❑ 1xADC 20bits@100Hz sampling frequency.
- ❑ 2xDAC 14Bit@200MHz conversion rate.
- ❑ 2 x programmable DC outputs (14 bit resolution).
- ❑ Real Time Bandwidth limiter via programmable 40-pole FIR filter on high speed input data stream.
- ❑ Embedded user interface for system control and signal monitoring.
- ❑ 5 ns trigger accuracy between captures on external input trigger.
- ❑ Integrated FPGA-based signal capture averaging functionality with up to 4095 signal cycles.
- ❑ Integrated FPGA-based FIR block . User programmable with up to 1023 taps with programmable decimation factor.
- ❑ Integrated FIR filter design tool. Free access to coefficient memory so the user can define their own filter coefficients (18 bits resolution).
- ❑ 4x digital output signals.Trigger-able.
- ❑ 4x digital input signals. Trigger-able.
- ❑ Integrated oscilloscope function. YT input signal representation on DVI standard VESA monitor (1280x1024 resolution). Selectable signal interpolation for 10ns/DIV, 25ns/DIV, 50ns/DIV and 125ns/DIV.
- ❑ Integrated DDS functionality on Analog and digital signals, fixed or arbitrary generation mode.

Specifications

ANALOG input 1
Sampling frequency: 400MHz
Bandwidth: 200MHz
ENOB/BW: 9Bits @100MHz
Base Noise: -68dBfs
Range: from +1.1V to -1.1V
Type: Single ended bipolar.
Input Impedance: 50 Ohm

ANALOG input 2 (AUX)
Sampling frequency: 100Hz
Bandwidth: 50Hz
*ENOB/BW: 18*Bits @25Hz
Range: from 0.65V to 2.85V
Type: Single ended Unipolar.
Input Impedance: 1KOhm

ANALOG outputs (HS)
Conversion rate: 200MHz
Bandwidth: 5MHz
*Resolution:*14 bits
Range: from -6V to 6V
Type: Single ended Bipolar.

ANALOG outputs (DC)
Range: from -6V to 6V
*Resolution:*14 bits
Type: Single ended Bipolar.

Digital inputs
Sampling frequency: 400MHz
Bandwidth: 200MHz
Range: from 0V to +5V
Type: Single ended
Input Impedance: 50 Ohm.

Digital Outputs
Update rate: 400MHz
Bandwidth: 200MHz
Range: from 0V to +5V
Type: Single ended

Logger Specs
Core: 32bit ARM processor + FPGAx3
Comm: Ethernet 10/100 Base-T
OSCI out : DVI 1280x1024 60Hz
Logger Memory: 1024MB SDRAM
Averaging Memory: 512MB SDRAM
Capture length: up to 300 ms
Capture rate: 2xcapture length
Average Cycles: 4095

Power Supply
8-24VDC, MAX 20W.

Dimensions
90mmx170mmx180mm.

Contact

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