PROTONV2-3M07
Hardware manual

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1 Features and architecture

The ramDSP Electronics PROTONV2-3M07 is a digital processing platform based on FPGA + microcontroller architecture optimized for parallel processing and multiple analog and digital IO handling applications. Next figure sketches the system architecture:

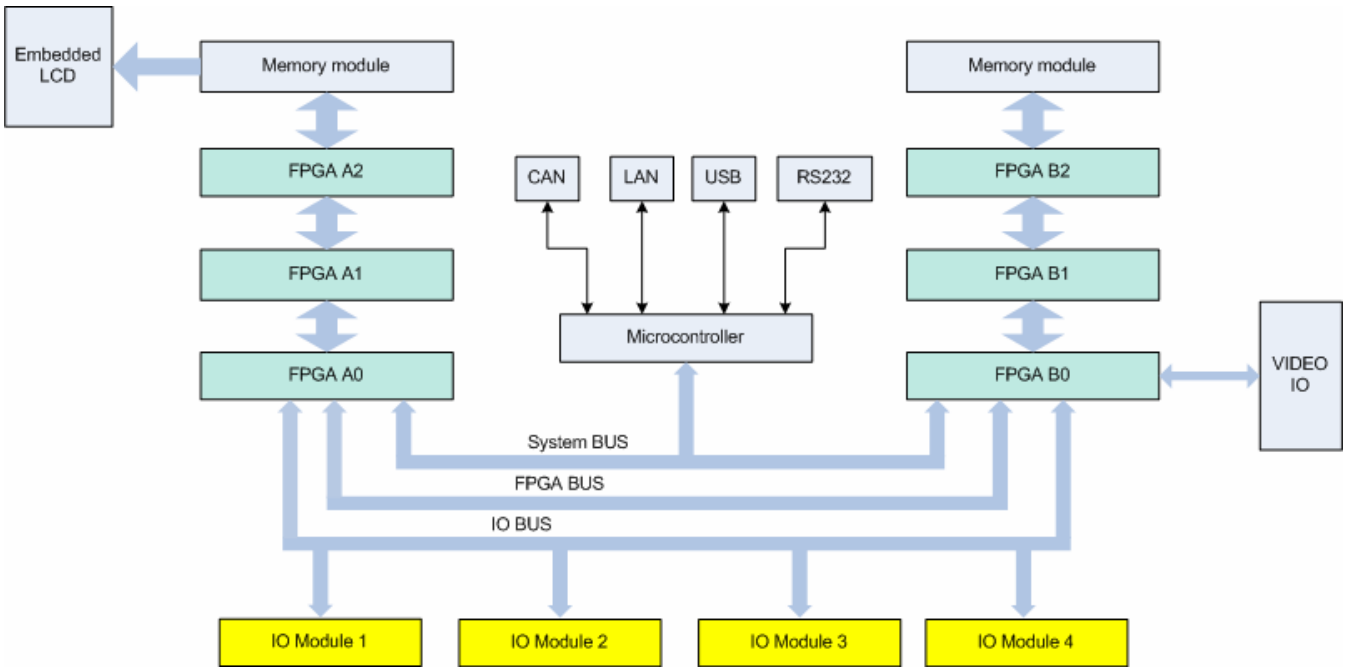

Figure 1. *PROTONV2-3M07 architecture*

- Up to 6 XILINX SPARTAN-III XC3S1500-4FG676C FPGA.
- Intel XSCALE PXA270 Microcontroller module. Integrates embedded NOR flash, SDRAM, SD card and communication resources (Ethernet, CAN, RS232…).
- 4 IO Module positions for user definable.
- Up to 512MB of SDRAM for video frame buffer directly controlled from FPGA.
- RGB Analog video input.
- Composite, Components analog video input.
- DVI input (single Link).
- DVI out put (Single Link).

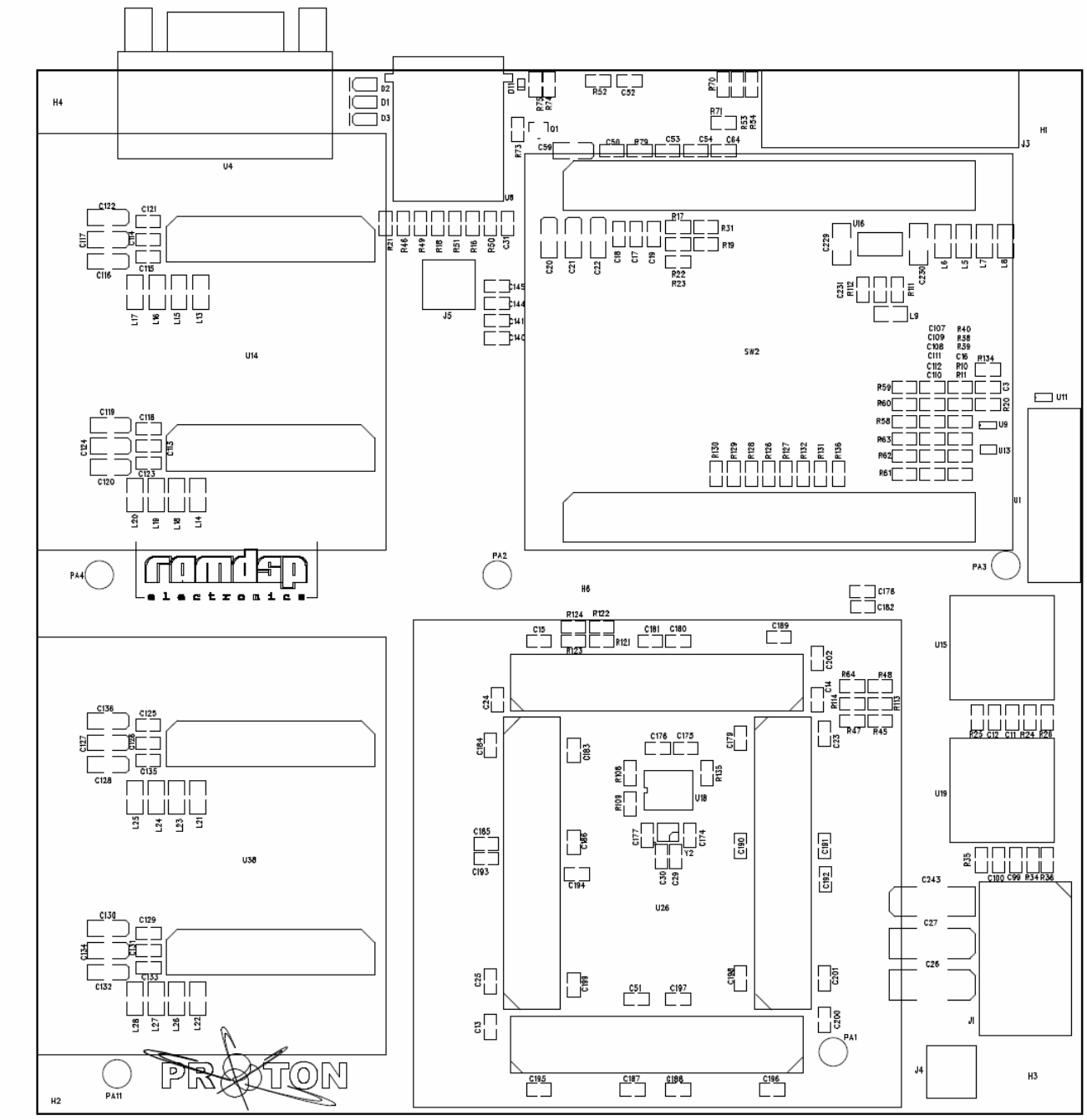

Figure 2. *Top Silkscreen of PROTONV2-3M07*

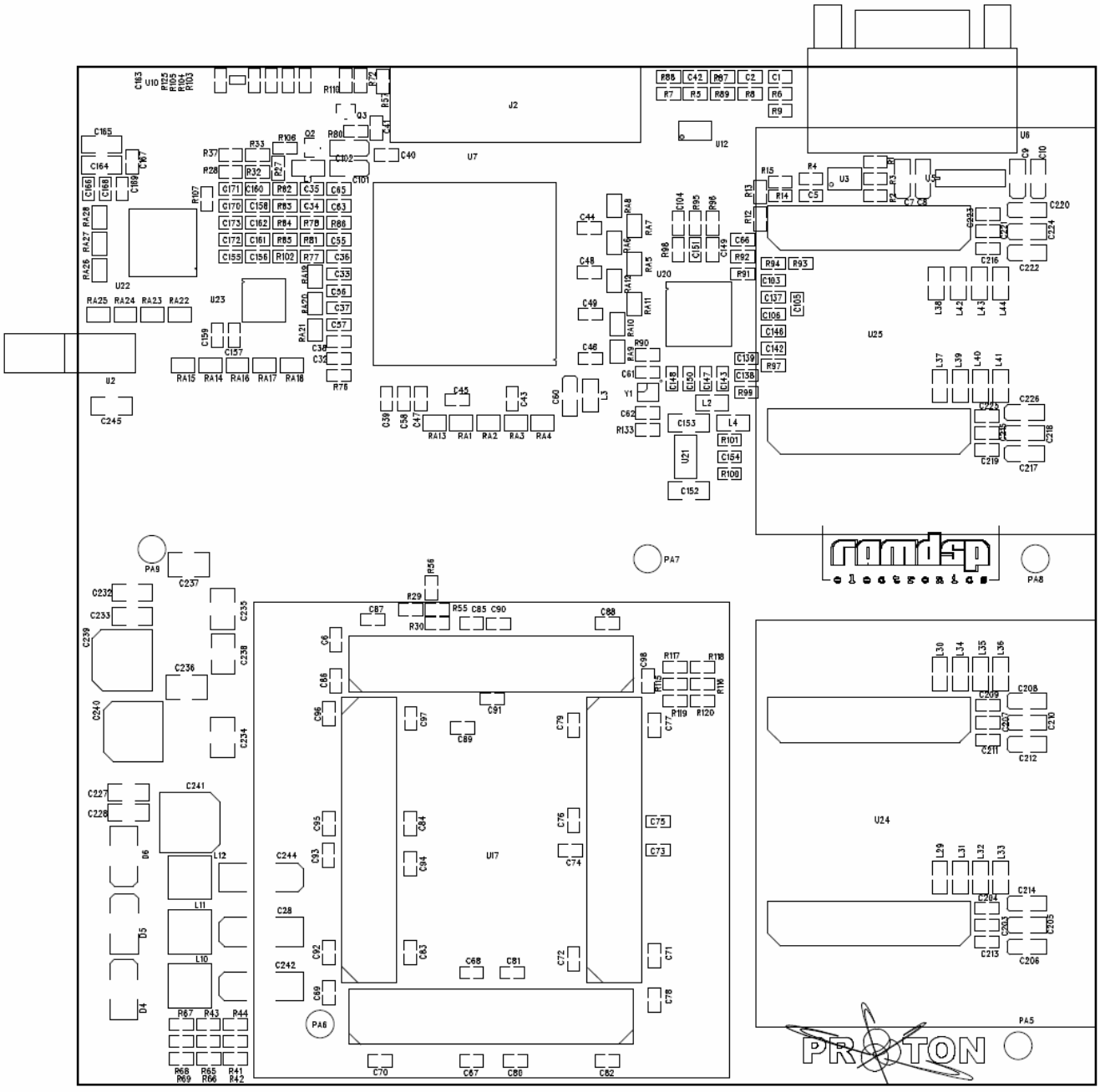

Figure 3. *Bottom Silkscreen of PROTONV2-3M07*

2 Microcontroller module

The Microcontroller module used in PROTONV2-3M07 is a 70mm x 57mm PCB. The module is powered with a single +3.3v power supply. It provides the following resources:

- Intel XSCALE PXA270 processor which including 3 UARTS, SPI bus controller, USB device controller, USB Host controller, MMC and SD card interface, LCD driver, Two wire interface I2C compatible and GPIO's.
- 64MB of SDRAM.
- 32MB of Flash memory.
- Ethernet MAC and PHY controller.
- CAN controller.

The microcontroller module in PROTONV2-3M07 is placed in the position labelled SW2. The following figure indicates the order of the microcontroller module connector pins and its relative position to other components on the PCB.

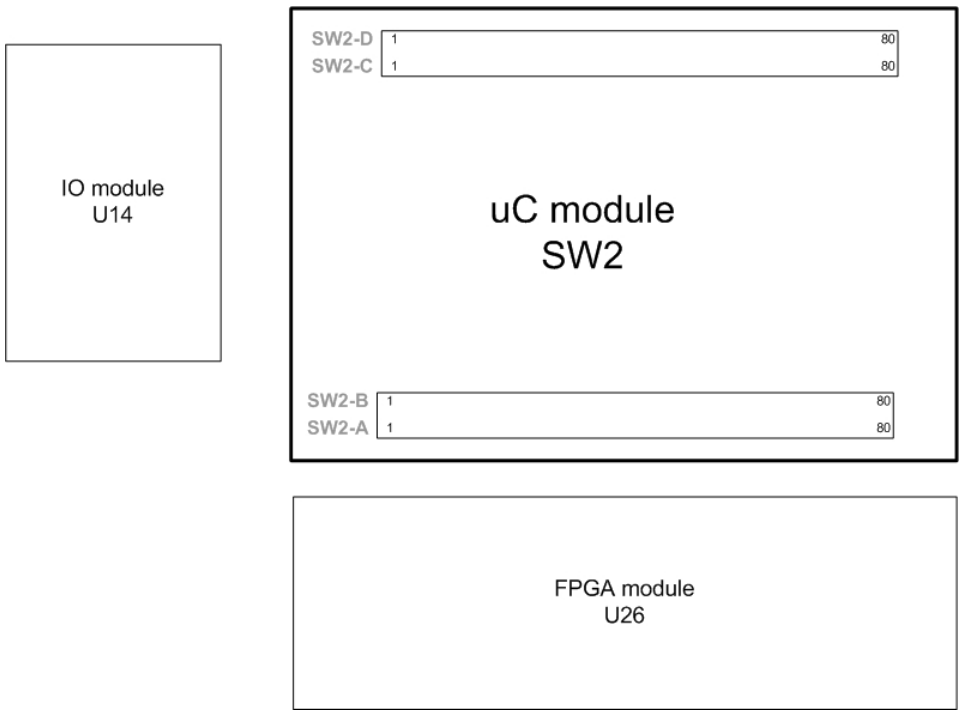

Figure 4. *Pin location of the microcontroller module on PROTONV2-3M07*

Next tables enumerate the pin assignment of the four pin rows distributed in two difference connectors used in the position SW2 (SW2-A, SW2-B, SW2-C and SW2-D).

Pin Number	Signal	I/O	Comments
SW2-A			
1A	CLKIN	I	Optional external clock input of the processor
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	CLK_REQ	I/O	Indicates Clocksource
4A	GPIO0	I/O	Processor I/O port, *alternative: interrupt*
5A	/CS_2	I/O	Freely available /CS signal of the processor, *alternative: GPIO78*
6A	/CS_4	I/O	Chip Select signal of the processor, *alternative: GPIO80*
8A	/WE	O	Write-enable signal for SDRAM, SRAM and Flash devices. Please note that the /PWE signal must be used for I/O components.
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A, 36A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23, A24	I/O	Address lines
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D1, D2, D4, D7, D9, D10, D12, D15, D18, D19, D20, D22, D25, D27, D28, D30	I/O	Data lines
34A, 35A	DQM_1, DQM_2	O	Byte enable signals
48A	RDY	I/O	Ready signal of the processor, *alternative: GPIO 18*
49A	RDnWR	O	Bus control singal of the processor

Pin Number	Signal	I/O	Comments
SW2-A			
50A, 51A	DREQ_0 DVAL_0	O	DMA request singal DREQ0 *alternative: GPIO 115* DVAL0 *alternative: GPIO 116*
53A,	/SDCKE_0	O	Clock enable for synchronous memory
55A, 56A	/SDCLK_0 /SDCLK_1	O	Clock signal for synchronous memory
58A, 59A	/PCE_1 /PCE_2	I/O	PCMCIA Chip Select resp. byte control signal, *alternative: GPIO85/54*
60A	/PWAIT	I/O	PCMCIA wait signal, *alternative: GPIO56*
61A	/IOIS16	I/O	PCMCIA 16-bit access *alternative: GPIO57*
63A	/PREG	I/O	PCMCIA register control signal *alternative: GPIO55*
64A	/LAN_CS	I	I/O Chip Select for LAN controller
65A	/LAN_DATA	I	DATA Chip Select for LAN controller
66A	L_VSYNC	O	Refresh sync signal from the LCD panel with internal frame buffer *alternative: GPIO14*
68A	L_PCLK	I/O	LCD pixel clock *alternative: GPIO76*
69A	L_LCLK	I/O	LCD line clock *alternative: GPIO75*
70A	L_FCLK	I/O	LCD frame clock *alternative: GPIO74*
71A	L_BIAS	I/O	LCD enable *alternative: GPIO77*
73A, 74A, 75A, 76A, 78A, 79A, 80A	L_DD3, L_DD5 L_DD6, L_DD8, L_DD11, L_DD13 L_DD14	I/O	LCD data *alternative: GPIO61, GPIO63, GPIO64, GPIO66, GPIO69, GPIO71, GPIO72*
SW2-B			
1B	nc		No connect
2B	nc		No connect
3B	GPIO_1	I/O	Processor I/O port, *alternative: interrupt*
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground 0 V
5B	nc		No connect

Pin Number	Signal	I/O	Comments
SW2-B			
6B	/CS_5	I/O	Chip Select signal of the processor, can be used to access the LAN controller, *alternative: GPIO33*
7B	/OE	O	Output-enable signal of the processor
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B 36B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22, A25	I/O	Address lines
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D0, D3, D5, D6, D8, D11, D13, D14, D16, D17, D21, D23, D24, D26, D29, D31	I/O	Data lines
33B, 35B	DQM_0, DQM_3	O	Byte enable signals
47B	/CS_0	O	Chip Select for on-board Flash
48B	/CS_1	I/O	/CS-Signal for second on-board 16-bit Flash, *alternative: GPIO15*
50B 51B 52B 53B	/SDCS_0 /SDCS_1 /SDCS_2, /SDCS_3	O O IO IO	/CS SDRAM bank #0 /CS SDRAM bank #1 /CS SDRAM bank #2 *alternative: GPIO20* /CS SDRAM bank #3 *alternative: GPIO21*
55B	/SDCLK_2	O	Clock signal for synchronous memory
56B	/SDRAS	O	/SDRAS control signal for SDRAM
57B	/SDCAS	O	/SDCAS control signal for SDRAM
58B	/PSKSEL	I/O	Card0/1 select *alternative: GPIO 79*
60B	/PWE	I/O	PCMCIA memory write signal and I/O write signal *alternative: GPIO 49*
61B	/POE	I/O	PCMCIA memory read signal *alternative: GPIO 48*
62B	/PIOR	I/O	PCMCIA I/O read signal *alternative: GPIO 50*
63B	/PIOW	I/O	PCMCIA I/O write signal *alternative: GPIO 51*
65B	/LAN_IRQ	I/O	Interrupt LAN controller
66B	L_CS	O	LCD CS *alternative: GPIO 19*
67B	L_DD16	O	LCD data *alternative: GPIO 86*
68B	L_DD17	O	LCD data *alternative: GPIO 87*

Pin Number	Signal	I/O	Comments
SW2-B			
70B, 71B, 72B, 73B, 75B, 76B 77B, 78B 80B	L_DD0, L_DD1, L_DD2, L_DD4, L_DD7, L_DD9, L_DD10, L_DD12, L_DD15	I/O	LCD data bus *alternative: GPIO 58, GPIO 59, GPIO 60, GPIO 65, GPIO 67, GPIO 68, GPIO 70, GPIO 73*
SW2-C			
1C, 2C	+3V3	P	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C 72C, 77C	GND	P	Ground 0 V
4C	VMMC	P	Optional supply voltage for internal MMC card
5C	VBAT	P	Input for external battery
6C	VCC_LCD	P	VCC for LCD Port
8C	USB_H_PWR	P	Over-current indicator from ports 3, 2 and 1
9C	Nc		No connect
10C	/RESIN	I/O	/Reset input for reset controller at U9
11C	/RESET_OUT	I/O	/Reset output of the PXA270 processor
13C	NSSP_TxD	I/O	Network SPI TxD signal, used for CAN Controller *Alternative: GPIO 81*
14C	NSSP_CLK	I/O	Network SPI Clock signal *Alternative: GPIO 84*
15C	NSSP_FRM	I/O	Network SPI Frame signal, used for CAN Controller *alternative: GPIO 83*
16C	NSSP_RxD	I/O	Network SPI RxD signal *Alternative: GPIO 82*
18C	IR_TXD	O	IrDA TxD *Alternative: GPIO 47*
19C	IR_RXD	I	IrDA RxD *Alternative: GPIO 46*
20C	FF_RI_DETECT	O	RI-Detect FF-UART (for interrupt)
21C	FF_/INVALID	O	Invalid level FF_UART
23C	/ACRESET	O	/RESET AC97 *Alternative: GPIO 113*
24C	SYNC	I/O	SYNC AC97 *Alternative: GPIO 31*

Pin Number	Signal	I/O	Comments
SW2-C			
25C	BITCLK	I/O	BITCLK *Alternative: GPIO 28*
26C	nc		No connect
28C	SDATA_IN_0	I/O	SDATA_IN0 (AC97 interface) *Alternative: GPIO 29*
29C	SDATA_OUT	I/O	SDATAOUT *Alternative: GPIO 30*
30C	SDA	I/O	I^2C data from processor *Alternative: GPIO 118*
31C	SCL	I	I^2C clock from processor *Alternative: GPIO 117*
33C	/LAN_LED_A-	O	LED A LAN controller, freely configurable
34C	/LAN_LED_B	O	LED B LAN-Controller, freely configurable
35C	LAN_TPI-	O	LAN negativer input
36C	LAN_TPO-	O	LAN negativer output
38C	OTG_ID	I	OTD ID Input USB Controller
39C	PWM0	O	PWM output #0 *Alternative: GPIO 16*
40C	PWM1	O	PWM output #1 *Alternative: GPIO 17*
41C	/TRST	O	JTAG reset
43C	USIM_IO	IO	USIM I/O Data. Receive and transmit data connection
44C	nc		No connect
45C	MMC_DAT2_CS0	O	MMC_C0 for external MMC card *Alternative: GPIO 110*
46C	MMC_DAT3_CS1	O	MMC_C1 for internal MMC card *Alternative: GPIO 111*
48C, 49C, 50C, 51C, 53C	GPIO114, GPIO9 GPIO10, GPIO12, GPIO90	I/O	GPIOs *Alternative: interrupt signals*

Pin Number	Signal	I/O	Comments
SW2-C			
54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C	EGPIO0, EGPIO1, EGPIO3, EGPIO6, EGPIO8, EGPIO9, EGPIO11, EGPIO14, EGPIO16, EGPIO17 EGPIO18, EGPIO22, EGPIO24 EGPIO25, EGPIO27	I/O	Additional GPIOs generated by the MAX7301 IC
73C	SSP_RXD	I	SPI RxD signal *Alternative: GPIO 26*
74C	SSP_TXD	O	SPI TxD signal *Alternative: GPIO 25*
75C	/CS_EGPIO	I	SSP /CS1 signal for MAX7301 (EGPIO)
76C	/CAN_CS	I	/CS signal for SJA1000 (CAN)
78C	/CAN_INT	O	CAN Interrupt
79C	CANRXD	I/O	CAN RxD signal
80C	CANTXD	I/O	CAN TxD signal
SW2-D			
1D, 2D	VCC	P	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND	-	Ground 0 V
4D, 5D	VCC1	P	Optional external supply voltage VCORE for processor, 3-5.0V
6D	VCC_BB	P	VCC Baseband
7D	USB_H_ENA	O	USB Controller Power Switch signal
8D	SYS_ENAB	O	System Power Switch signal
10D	/RESET	O	Reset output from reset controller
11D	/BATT_FAULT	I	Low battery voltage indication
12D	/VCC_FAULT	I	Low supply voltage indication
13D	PWR_ENAB	O	PXA-Core Power Signal
15D	BT_CTS	I	CTS Bluetooth UART *Alternative: GPIO 44*
16D	BT_RXD	I	RXD Bluetooth UART *Alternative: GPIO 42*

Pin Number	Signal	I/O	Comments
SW2-D			
17D	BT_TXD	O	TXD Bluetooth UART *Alternative: GPIO 43*
18D	BT_RTS	O	RTS Bluetooth UART *Alternative: GPIO 45*
20D	FF_/SHDN	I	FF-UART power on
21D	FL_WP_PEN	I	Flash Write Protect
22D	RS_RXD	I	FF-UART RxD signal (RS-232)
23D	RS_TXD	O	FF-UART TxD signal (RS-232)
25D	RS_RTS	I	FF-UART RTS signal (RS-232)
26D	RS_CTS	I	FF-UART CTS signal (RS-232)
27D	RS_DSR	I	FF-UART DSR signal (RS-232)
28D	RS_DTR	O	FF-UART DTR signal (RS-232)
30D	RS_RI	I	FF-UART RI signal (RS-232)
31D	RS_DCD	I	FF-UART DCD signal (RS-232)
32D	USB_C_P	I/O	USB Client positive, from processor
33D	USB_C_N	I/O	USB Client negative, from processor
35D	LAN_TPI+	O	LAN input positive
36D	LAN_TPO+	O	LAN output positive
37D	USB_H _P	I/O	USB Host Controller positive, from processor
38D	USB_H_N	I/O	USB Host Controller negative, from processor
40D	TDI	I	JTAG TDI signal
41D	TDO	O	JTAG TDO signal
42D	TMS	I	JTAG TMS signal
43D	TCK	I	JTAG TCK signal
45D	MMC_CLK	I/O	MMC_CLK signal
46D	MMC_DAT0	I/O	MMC_DAT signal
47D	MMC_CMD	I/O	MMC_CMD signal
48D	MMC_DAT1	I/O	MMC_DAT1 signal
50D, 51D, 52D, 53D	GPIO11, GPIO13, GPIO52, GPIO91,	I/O	GPIOs, *alternative: interrupt signals*
55D, 56D, 57D, 58D, 60D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D	EGPIO2, EGPIO4, EGPIO5, EGPIO7 EGPIO10, EGPIO12, EGPIO13, EGPIO15, EGPIO19, EGPIO20, EGPIO21, EGPIO23, EGPIO26	I/O	Additional GPIOs generated by the MAX7301 IC with 7 interrupt-capable inputs for connection to a matrix keyboard

Pin Number	Signal	I/O	Comments
SW2-D			
71D	SSP_EXTCLK	I	SPI external clock *alternative: GPIO 27*
72D	SSP_CLK	O	SPI clock signal *alternative: GPIO 23*
73D	SSP_SFRM	I/O	SPI frame signal *alternative: GPIO 24*
75D	FL_DIS	I	Signal to disable internal Flash
76D	SSP_SYSCLK	I/O	SYSCLOCK SSP *Alternative: GPIO 53*
77D	PWR_SDA	I/O	Power I2C Serial Data/Address signal *Alternative: GPIO 4*
78D	PWR_SCL	O	Power I2C Serial Clock Line signal *Alternative: GPIO 3*
80D	/INT_RTC	O	Interrupt output RTC

3 FPGA's

Two connector areas (U26 and U17) are dedicated to plug stackable FPGA modules

3.1 FPGA configuration

The FPGA's on PROTONV2-3M07 can be configured from three different sources:

- Via JTAG bus.
- From the microcontroller of the system (parallel or serial Slave modes).
- From the configuration EEPROM present on every FPGA module (Serial master mode).

The supported FPGA configuration modes are listed in the following table.

Mode	M0	M1	M2	Description
Master Serial	0	0	0	Supported. Configuration bitstream is loaded from PROM (default set by pull-down resistors).
Slave Serial	1	1	1	Supported. The Configuration bitstream is loaded from the uC.
Master Parallel	*1*	*1*	*0*	*Not supported.*
Slave Parallel	0	1	1	Supported. The Configuration bitstream is loaded from the uC.
JTAG	1	0	1	The FPGA is programmed through JTAG port

3.1.1 JTAG

See JTAG chain section.

3.1.2 Microcontroller

The microcontroller of the system can configure the FPGA's on PROTONV2 using two different programming modes:

- Parallel Slave mode (SelectMap).
- Serial Slave mode.

The configuration modes of both FPGA locations can be set up with the same microcontroller GPIO's. Each mode signals of the FPGA can be isolated independently removing the right zero ohm resistor. Next table describes the connections between microcontroller and FPGA programming mode pins.

	FPGA 1 (U26)		FPGA 2 (U17)		Microcontroller	
	resistor	Net	resistor	Net	GPIO	NET
M0	R47	M0_FPGA1	R116	M0_FPGA2	GPIO9	ARM_GPIO9

	FPGA 1 (U26)		FPGA 2 (U17)		Microcontroller	
	resistor	Net	resistor	Net	GPIO	NET
M1	R64	M1_FPGA1	R118	M1_FPGA2	GPIO10	ARM_GPIO10
M2	R114	M2_FPGA1	R120	M2_FPGA2	GPIO11	ARM_GPIO11

FPGA programming control signals are assigned independently for each FPGA block. The next two tables show the connection between microcontroller and FPGA's.

FPGA 1 configuration control signals (U26)					
FPGA 1 (U26)			Microcontroller		
	Pin	Net	GPIO	NET	Option
DOUT	AD14	BK4_IO_P2/DOUT	GPIO113	ARM_#ACRESET	--
INITB	AC14	BK4_IO_N2/INITB	GPIO31	ARM_SYNC	--
RDWR_B	AC5	BK4_IO_N25/RDWR_B	GPIO28	ARM_BITCLK	--
PROG_B	--	PROGB	GPIO90	ARM_GPIO90	--
DONE	--	DONE	GPIO91	ARM_GPIO91	--
CCLK	--	CCLK	--	ARM_#WE	if R29 populated
			GPIO49	ARM_#PWE	if R30 populated (default)
CS_B	AB5	BK4_IO_P25/CS_B	GPIO78	ARM_#CS2	if R55 populated
			GPIO55	ARM_#PREG	if R56 populated (default)

FPGA 2 configuration control signals (U17)					
FPGA 2 (U17)			Microcontroller		
	Pin	Net	GPIO	NET	Option
DOUT	AD14	BK4_IO_P2/DOUT	GPIO1	ARM_GPIO1	--
INITB	AC14	BK4_IO_N2/INITB	GPIO26	#INIT_FPGA_2	--
RDWR_B	AC5	BK4_IO_N25/RDWR_B	GPIO84	RD/#RW_FPGA_2	--
PROG_B	--	PROGB	GPIO83	#PROG_FPGA_2	Used for CAN controller
DONE	--	DONE	GPIO81	DONE_FPGA_2	Used for CAN controller
CCLK	--	CCLK	--	ARM_#WE	if R29 populated
			GPIO49	ARM_#PWE	if R30 populated (default)
CS_B	AB5	BK4_IO_P25/CS_B	GPIO78	ARM_#CS2	if R55 populated
			GPIO55	ARM_#PREG	if R56 populated (default)

The FPGA programming data signals of both FPGA's are part of the system bus and are connected together. D0 programming data signal can be used only as an input after programming when the mode pins select a slave programming mode.

FPGA 1 and 2 data signals (U26/U17)					
FPGA 1 and 2 (U26/U17)			Microcontroller		
	Pin	Net	GPIO	NET	Description
D0	Y15	BK4_IO_N6/D0_C	--	ARM_D00	Used in Parallel and serial modes
D1	W14	BK4_IO_P6/D1	--	ARM_D01	Used in Parallel mode
D2	Y14	BK4_IO_N3/D2	--	ARM_D02	Used in Parallel mode
D3	AA14	BK4_IO_P3/D3	--	ARM_D03	Used in Parallel mode
D4	AC13	BK4_IO_N2/D4	--	ARM_D04	Used in Parallel mode
D5	AB13	BK4_IO_P2/D5	--	ARM_D05	Used in Parallel mode
D6	AB12	BK4_IO_N5/D6	--	ARM_D06	Used in Parallel mode
D7	AA12	BK4_IO_P5/D7	--	ARM_D07	Used in Parallel mode

3.1.3 Configuration EEPROM

Every FPGA module contain a programming EEPROM. These EEPROM's can only be programmed via JTAG. For loading the FPGA bit stream from the EEPROM to the FPGA the master serial programming mode has to be selected using (M0, M1 and M2). By asserting low for 100us the PROGB signal of the each FPGA, the configuration bit stream present in the EEPROM is loaded into the FPGA. The INITB pin can be used to delay the configuration process. For more info about configuration processes on XILINX FPGA refer to the corresponding data sheets and application notes.

3.2 FPGA modules pin assignment

Next figure shows the position of the FPGA connectors on the top side of PROTONV2-3M07.

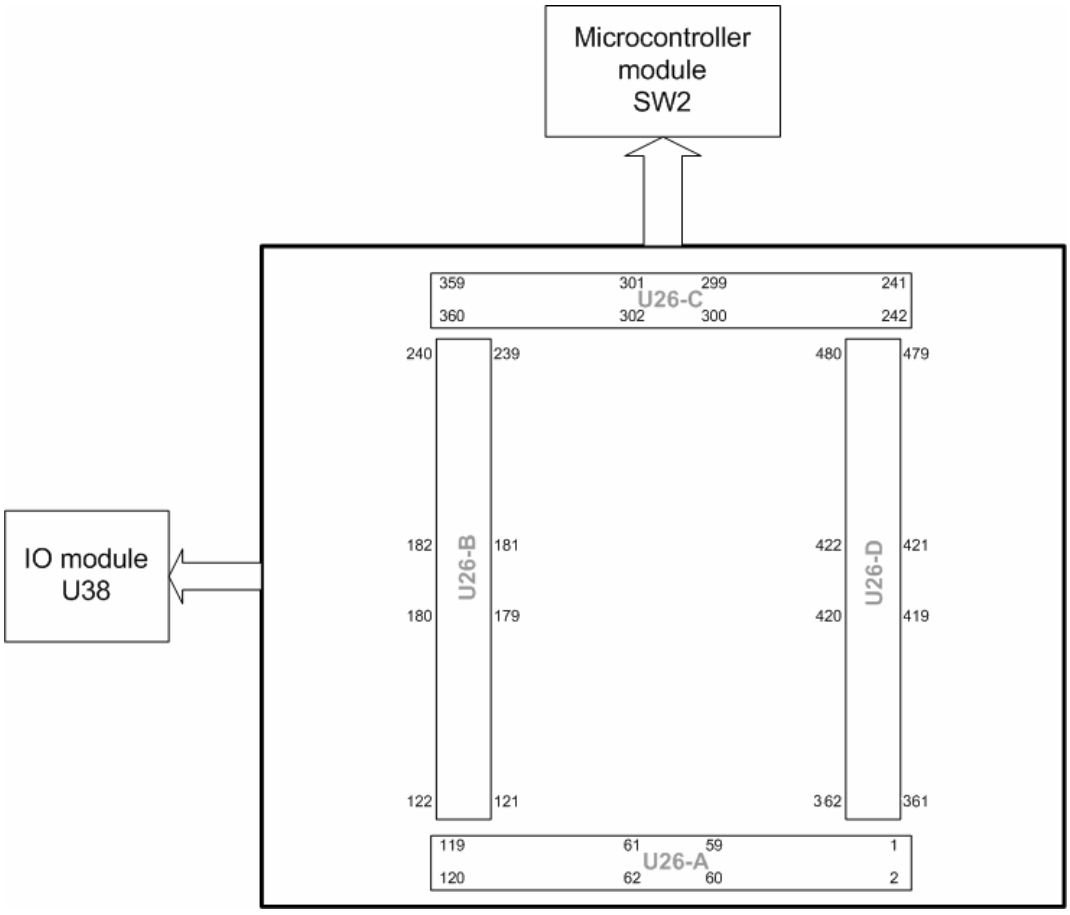

Figure 5. *FPGA module pin locations for position U26 (Top layer)*

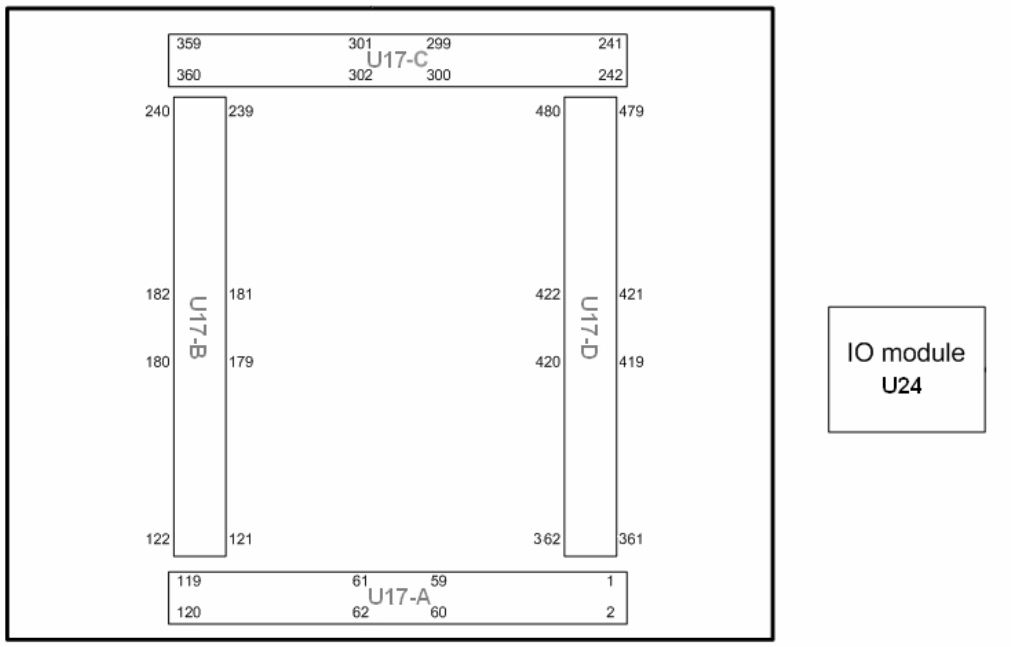

Figure 6. *FPGA module pin locations for position U17 (Bottom layer)*

3.2.1 FPGA 1 (U26)

The connectors U26-A, U26-B, U26-C and U26-D are SAMTEC QSH-060-02-L-D-A connected targeted for the ramDSP electronics ERIZOV0-XC3S1500 FPGA module. Next tables enumerate the pin assignment of the connectors for the FPGA module placed on position U26.

Connector U26-A	**FPGA**		**Description**	
Pin	Pin	Name	Net name	Function
1	--	+3.3v	+3.3v power supply	
2	--	+3.3v		
3	--	GND	Ground	
4	--	GND		
5	E5	BK0_IO_N25/VRP	IO2_DB30	data line 30 of bus B for IO module 2
6	B3	BK0_IO_S12/VREF	IO2_DB27	data line 27 of bus B for IO module 2
7	D5	BK0_IO_P25/VRN	IO2_DB28	data line 28 of bus B for IO module 2
8	A3	BK0_IO_S11	IO2_DB25	data line 25 of bus B for IO module 2
9	C5	BK0_IO_N23	IO2_DB26	data line 26 of bus B for IO module 2
10	C4	BK0_IO_S10	IO2_DB23	data line 23 of bus B for IO module 2
11	B5	BK0_IO_P23	IO2_DB24	data line 4 of bus B for IO module 2
12	A4	BK0_IO_P24/VREF	IO2_DB21	data line 21 of bus B for IO module 2
13	C6	BK0_IO_N21	IO2_DB22	data line 22 of bus B for IO module 2
14	B4	BK0_IO_N24	IO2_DB19	data line 19 of bus B for IO module 2
15	B6	BK0_IO_P21	IO2_DB20	data line 20 of bus B for IO module 2
16	A5	BK0_IO_S9	IO2_DB17	data line 17 of bus B for IO module 2
17	E7	BK0_IO_N20	IO2_DB18	data line 18 of bus B for IO module 2
18	C8	BK0_IO_S6*	IO2_DB15	data line 15 of bus B for IO module 2
19	D7	BK0_IO_P20	IO2_DB16	data line 16 of bus B for IO module 2
20	A6	BK0_IO_S8	IO2_DB13	data line 13 of bus B for IO module 2
21	E6	BK0_IO_N22	IO2_DB14	data line 14 of bus B for IO module 2
22	B7	BK0_IO_N19	IO2_DB11	data line 11 of bus B for IO module 2
23	D6	BK0_IO_P22	IO2_DB12	data line 12 of bus B for IO module 2
24	A7	BK0_IO_P19	IO2_DB09	data line 9 of bus B for IO module 2
25	F7	BK0_IO_S7/VREF	IO2_DB10	data line 10 of bus B for IO module 2
26	B8	BK0_IO_N16	IO2_DB07	data line 7 of bus B for IO module 2

Connector U26-A	FPGA		Description	
Pin	Pin	Name	Net name	Function
27	E8	BK0_IO_N17*	IO2_DB08	data line 8 of bus B for IO module 2
28	A8	BK0_IO_P16	IO2_DB05	data line 5 of bus B for IO module 2
29	D8	BK0_IO_P17*	IO2_DB06	data line 6 of bus B for IO module 2
30	C12	BK0_IO_S2	IO2_DB03	data line 3 of bus B for IO module 2
31	G8	BK0_IO_N18*	IO2_DB04	data line 4 of bus B for IO module 2
32	B10	BK0_IO_N10*	IO2_DB01	data line 1 of bus B for IO module 2
33	F8	BK0_IO_P18*	IO2_DB02	data line 2 of bus B for IO module 2
34	A10	BK0_IO_P10*	IO2_DA49	data line 49 of bus A for IO module 2
35	E9	BK0_IO_N14*	IO2_DB00	data line 0 of bus B for IO module 2
36	B11	BK0_IO_N7*	IO2_DA47	data line 47 of bus A for IO module 2
37	D9	BK0_IO_P14*	IO2_DA48	data line 48 of bus A for IO module 2
38	A11	BK0_IO_P7/VREF*	IO2_DA45	data line 45 of bus A for IO module 2
39	C9	BK0_IO_N13*	IO2_DA46	data line 46 of bus A for IO module 2
40	B12	BK0_IO_N4	IO2_DA43	data line 43 of bus A for IO module 2
41	B9	BK0_IO_P13*	IO2_DA44	data line 44 of bus A for IO module 2
42	A12	BK0_IO_P4	IO2_DA41	data line 41 of bus A for IO module 2
43	G9	BK0_IO_N15	IO2_DA42	data line 42 of bus A for IO module 2
44	B13	BK0_IO_N1/CLK7	PIX_CLK_Y0	output clock 0 from CDC706 PLL
45	F9	BK0_IO_P15	IO2_DA40	data line 40 of bus A for IO module 2
46	A13	BK0_IO_P1/CLK6	IO1_DB11	data line 11 of bus B for IO module 1
47	G10	BK0_IO_S5/VREF	IO2_DA38	data line 38 of bus A for IO module 2
48	D11	BK0_IO_P8	IO2_DA39	data line 39 of bus A for IO module 2
49	F10	BK0_IO_N12	IO2_DA36	data line 36 of bus A for IO module 2
50	E11	BK0_IO_N8	IO2_DA37	data line 37 of bus A for IO module 2
51	E10	BK0_IO_P12	IO2_DA34	data line 34 of bus A for IO module 2
52	G11	BK0_IO_N9	IO2_DA35	data line 35 of bus A for IO module 2
53	D10	BK0_IO_N11	IO2_DA32	data line 32 of bus A for IO module 2
54	F11	BK0_IO_P9	IO2_DA33	data line 33 of bus A for IO module 2
55	C10	BK0_IO_P11	IO2_DA30	data line 30 of bus A for IO module 2
56	H12	BK0_IO_S3	IO2_DA31	data line 31 of bus A for IO module 2
57	--	GND	Ground	
58	--	GND		
59	--	VCC_0	Power supply for FPGA IO bank 0 and bank 1	
60	--	VCC_0		
61	--	VCC_1		
62	--	VCC_1		
63	--	GND	Ground	
64	--	GND		
65	H11	BK0_IO_S4	IO2_DA28	data line 28 of bus A for IO module 2
66	E13	BK0_IO_S1	IO2_DA29	data line 29 of bus A for IO module 2
67	G12	BK0_IO_N6	IO2_DA26	data line 26 of bus A for IO module 2
68	C13	BK0_IO_P2/VREF	IO2_DA27	data line 27 of bus A for IO module 2
69	H13	BK0_IO_P6	IO2_DA24	data line 24 of bus A for IO module 2
70	D13	BK0_IO_N2	IO2_DA25	data line 25 of bus A for IO module 2
71	H14	BK1_IO_P3	IO2_DA22	data line 22 of bus A for IO module 2
72	C15	BK1_IO_S3/VREF	IO2_DA23	data line 23 of bus A for IO module 2
73	G14	BK1_IO_N3	IO2_DA20	data line 20 of bus A for IO module 2
74	A14	BK1_IO_S1	IO2_DA21	data line 21 of bus A for IO module 2
75	F12	BK0_IO_N5	IO2_DA18	data line 18 of bus A for IO module 2
76	B15	BK1_IO_P4	IO2_DA19	data line 19 of bus A for IO module 2
77	E12	BK0_IO_P5	IO2_DA16	data line 16 of bus A for IO module 2
78	A15	BK1_IO_N4	IO2_DA17	data line 17 of bus A for IO module 2
79	F13	BK0_IO_P3	IO2_DA14	data line 14 of bus A for IO module 2
80	B16	BK1_IO_P7*	IO2_DA15	data line 15 of bus A for IO module 2
81	G13	BK0_IO_N3	IO2_DA12	data line 12 of bus A for IO module 2
82	A16	BK1_IO_N7*	IO2_DA13	data line 13 of bus A for IO module 2
83	F14	BK1_IO_S2	IO2_DA10	data line 10 of bus A for IO module 2
84	B17	BK1_IO_P10*	IO2_DA11	data line 11 of bus A for IO module 2
85	D14	BK1_IO_N2/VREF	IO2_DA08	data line 8 of bus A for IO module 2
86	A17	BK1_IO_N10*	IO2_DA09	data line 9 of bus A for IO module 2
87	E14	BK1_IO_P2	IO2_DA06	data line 6 of bus A for IO module 2
88	C17	BK1_IO_S5/VREF	IO2_DA07	data line 7 of bus A for IO module 2
89	F15	BK1_IO_P5	IO2_DA04	data line 4 of bus A for IO module 2
90	B19	BK1_IO_P15	IO2_DA05	data line 5 of bus A for IO module 2
91	E15	BK1_IO_N5	IO2_DA02	data line 2 of bus A for IO module 2
92	A19	BK1_IO_N15	IO2_DA03	data line 3 of bus A for IO module 2
93	G16	BK1_IO_N9	IO2_DA00	data line 0 of bus A for IO module 2
94	B20	BK1_IO_P18	IO2_DA01	data line 1 of bus A for IO module 2
95	H16	BK1_IO_P9	IO1_DB48	data line 48 of bus B for IO module 1

Connector U26-A	FPGA		Description	
Pin	Pin	Name	Net name	Function
96	A20	BK1_IO_N18/VREF	IO1_DB49	data line 49 of bus B for IO module 1
97	F17	BK1_IO_N12	IO1_DB46	data line 46 of bus B for IO module 1
98	B21	BK1_IO_P20	IO1_DB47	data line 47 of bus B for IO module 1
99	G17	BK1_IO_P12	IO1_DB44	data line 44 of bus B for IO module 1
100	A21	BK1_IO_N20	IO1_DB45	data line 45 of bus B for IO module 1
101	F18	BK1_IO_N14	IO1_DB42	data line 42 of bus B for IO module 1
102	A22	BK1_IO_S10	IO1_DB43	data line 43 of bus B for IO module 1
103	G18	BK1_IO_P14	IO1_DB40	data line 40 of bus B for IO module 1
104	D18	BK1_IO_S6/VREF*	IO1_DB41	data line 41 of bus B for IO module 1
105	F19	BK1_IO_P17*	IO1_DB38	data line 38 of bus B for IO module 1
106	A23	BK1_IO_S11	IO1_DB39	data line 39 of bus B for IO module 1
107	E19	BK1_IO_N17*	IO1_DB37	data line 37 of bus B for IO module 1
108	--	GND	Ground	
109	G19	BK1_IO_S8	IO1_DB36	data line 36 of bus B for IO module 1
110	--	TDI	TDI_FPGA1	JTAG data input
111	F20	BK1_IO_S9	IO1_DB35	data line 35 of bus B for IO module 1
112	--	TDO	TDO_FPGA1	JTAG data output
113	F21	BK1_IO_P23	IO1_DB34	data line 34 of bus B for IO module 1
114	--	TMS	TMS	JTAG chip select
115	E21	BK1_IO_N23	IO1_DB33	data line 33 of bus B for IO module 1
116	--	TCK	TCK	JTAG clock signal
117	--	GND	Ground	
118	--	GND		
119	--	+3.3v	+3.3v power supply	
120	--	+3.3v		

Connector U26-B	FPGA		Description	
Pin	Pin	Name	Net Name	Function
121	--	+3.3v	+3.3v power supply	
122	--	+3.3v		
123	--	GND	Ground	
124	--	GND		
125	C18	BK1_IO_P13*	IO1_DA00	data line 0 of bus A for IO module 1
126	G15	BK1_IO_N6	IO1_DA01	data line 1 of bus A for IO module 1
127	B18	BK1_IO_N13*	IO1_DA02	data line 2 of bus A for IO module 1
128	H15	BK1_IO_P6	IO1_DA03	data line 3 of bus A for IO module 1
129	D19	BK1_IO_P16*	IO1_DA04	data line 4 of bus A for IO module 1
130	F16	BK1_IO_P8	IO1_DA05	data line 5 of bus A for IO module 1
131	C19	BK1_IO_N16*	IO1_DA06	data line 6 of bus A for IO module 1
132	E16	BK1_IO_N8	IO1_DA07	data line 7 of bus A for IO module 1
133	D20	BK1_IO_N19	IO1_DA08	data line 8 of bus A for IO module 1
134	D16	BK1_IO_S4	IO1_DA09	data line 9 of bus A for IO module 1
135	E20	BK1_IO_P19	IO1_DA10	data line 10 of bus A for IO module 1
136	D17	BK1_IO_N11	IO1_DA11	data line 11 of bus A for IO module 1
137	C21	BK1_IO_N21	IO1_DA12	data line 12 of bus A for IO module 1
138	E17	BK1_IO_P11	IO1_DA13	data line 13 of bus A for IO module 1
139	D21	BK1_IO_P21	IO1_DA14	data line 14 of bus A for IO module 1
140	E18	BK1_IO_S7	IO1_DA15	data line 15 of bus A for IO module 1
141	B22	BK1_IO_N22/VREF	IO1_DA16	data line 16 of bus A for IO module 1
142	C25	BK2_IO_N1/VRP	IO1_DA17	data line 17 of bus A for IO module 1
143	C22	BK1_IO_P22	IO1_DA18	data line 18 of bus A for IO module 1
144	C26	BK2_IO_P1/VRN	IO1_DA19	data line 19 of bus A for IO module 1
145	B23	BK1_IO_N24	IO1_DA20	data line 20 of bus A for IO module 1
146	D25	BK2_IO_N3/VREF	IO1_DA21	data line 21 of bus A for IO module 1
147	C23	BK1_IO_P24	IO1_DA22	data line 22 of bus A for IO module 1
148	D26	BK2_IO_P3	IO1_DA23	data line 23 of bus A for IO module 1
149	D22	BK1_IO_N25/VRP	IO1_DA24	data line 24 of bus A for IO module 1
150	E25	BK2_IO_N4*	IO1_DA25	data line 25 of bus A for IO module 1
151	E22	BK1_IO_P25/VRN	IO1_DA26	data line 26 of bus A for IO module 1
152	E26	BK2_IO_P4*	IO1_DA27	data line 27 of bus A for IO module 1
153	E23	BK2_IO_N2	IO1_DA28	data line 28 of bus A for IO module 1
154	F25	BK2_IO_N8/VREF*	IO1_DA29	data line 29 of bus A for IO module 1
155	E24	BK2_IO_P2	IO1_DA30	data line 30 of bus A for IO module 1
156	F26	BK2_IO_P8*	IO1_DA31	data line 31 of bus A for IO module 1
157	F23	BK2_IO_N6*	IO1_DA32	data line 32 of bus A for IO module 1
158	G25	BK2_IO_N9*	IO1_DA33	data line 33 of bus A for IO module 1

Connector U26-B	FPGA		Description	
Pin	Pin	Name	Net Name	Function
159	F24	BK2_IO_P6*	IO1_DA34	data line 34 of bus A for IO module 1
160	G26	BK2_IO_P9*	IO1_DA35	data line 35 of bus A for IO module 1
161	K20	BK2_IO_P14	IO1_DA36	data line 36 of bus A for IO module 1
162	H25	BK2_IO_N13	IO1_DA37	data line 37 of bus A for IO module 1
163	J20	BK2_IO_N14	IO1_DA38	data line 38 of bus A for IO module 1
164	H26	BK2_IO_P13	IO1_DA39	data line 39 of bus A for IO module 1
165	J22	BK2_IO_N15	IO1_DA40	data line 40 of bus A for IO module 1
166	K25	BK2_IO_N19	IO1_DA41	data line 41 of bus A for IO module 1
167	J23	BK2_IO_P15	IO1_DA42	data line 42 of bus A for IO module 1
168	K26	BK2_IO_P19	IO1_DA43	data line 43 of bus A for IO module 1
169	K21	BK2_IO_N17/VREF	IO1_DA44	data line 44 of bus A for IO module 1
170	L25	BK2_IO_N22	IO1_DA45	data line 45 of bus A for IO module 1
171	K22	BK2_IO_P17	IO1_DA46	data line 46 of bus A for IO module 1
172	L26	BK2_IO_P22	IO1_DA47	data line 47 of bus A for IO module 1
173	L21	BK2_IO_N21	IO1_DA48	data line 48 of bus A for IO module 1
174	M25	BK2_IO_N26/VREF	IO1_DA49	data line 49 of bus A for IO module 1
175	L22	BK2_IO_P21	IO1_DB00	data line 0 of bus B for IO module 1
176	M26	BK2_IO_P26	IO1_DB01	data line 1 of bus B for IO module 1
177	--	GND	Ground	
178	--	GND		
179	--	VCC_2	+3.3V power supply applied to bank 2	
180	--	VCC_2		
181	--	VCC_3	+3.3V power supply applied to bank 3	
182	--	VCC_3		
183	--	GND	Ground	
184	--	GND		
185	N22	BK2_IO_P28	IO1_DB02	data line 2 of bus B for IO module 1
186	N25	BK2_IO_N30	IO1_DB03	data line 3 of bus B for IO module 1
187	N21	BK2_IO_N28	IO1_DB04	data line 4 of bus B for IO module 1
188	N26	BK2_IO_P30/VREF	IO1_DB05	data line 5 of bus B for IO module 1
189	K24	BK2_IO_P18	IO1_DB06	data line 6 of bus B for IO module 1
190	G20	BK2_IO_N5*	IO1_DB07	data line 7 of bus B for IO module 1
191	K23	BK2_IO_N18	IO1_DB08	data line 8 of bus B for IO module 1
192	G21	BK2_IO_P5*	IO1_DB09	data line 9 of bus B for IO module 1
193	M19	BK2_IO_N23	IO1_DB10	data line 10 of bus B for IO module 1
194	**F22**	**BK2_IO_S1****	**GND**	**Not present in XC3S1500**
195	M20	BK2_IO_P23	IO1_DB12	data line 12 of bus B for IO module 1
196	H20	BK2_IO_N10	IO1_DB13	data line 13 of bus B for IO module 1
197	N20	BK2_IO_P27	IO1_DB14	data line 14 of bus B for IO module 1
198	H21	BK2_IO_P10	IO1_DB15	data line 15 of bus B for IO module 1
199	N19	BK2_IO_N27	IO1_DB16	data line 16 of bus B for IO module 1
200	J21	BK2_IO_P11	IO1_DB17	data line 17 of bus B for IO module 1
201	M22	BK2_IO_P24	IO1_DB18	data line 18 of bus B for IO module 1
202	H22	BK2_IO_N11	IO1_DB19	data line 19 of bus B for IO module 1
203	M21	BK2_IO_N24	IO1_DB20	data line 20 of bus B for IO module 1
204	G22	BK2_IO_N7*	IO1_DB21	data line 21 of bus B for IO module 1
205	L20	BK2_IO_P20	IO1_DB22	data line 22 of bus B for IO module 1
206	G23	BK2_IO_P7*	IO1_DB23	data line 23 of bus B for IO module 1
207	L19	BK2_IO_N20	IO1_DB24	data line 24 of bus B for IO module 1
208	H24	BK2_IO_P12/VREF	IO1_DB25	data line 25 of bus B for IO module 1
209	--	NC	Not connected	
210	H23	BK2_IO_N12	IO1_DB26	data line 26 of bus B for IO module 1
211	--	NC	Not connected	
212	J24	BK2_IO_N16	IO1_DB27	data line 27 of bus B for IO module 1
213	--	NC	Not connected	
214	J25	BK2_IO_P16	IO1_DB28	data line 28 of bus B for IO module 1
215	--	NC	Not connected	
216	M24	BK2_IO_P25	IO1_DB29	data line 29 of bus B for IO module 1
217	--	NC	Not connected	
218	L23	BK2_IO_N25	IO1_DB30	data line 30 of bus B for IO module 1
219	--	NC	Not connected	
220	N24	BK2_IO_P29	IO1_DB31	data line 31 of bus B for IO module 1
221	--	NC	Not connected	
222	N23	BK2_IO_N29	IO1_DB32	data line 32 of bus B for IO module 1
223	--	NC	Not connected	
224	--	NC	Not connected	
225	--	NC	Not connected	
226	--	NC	Not connected	
227	--	NC	Not connected	

Connector U26-B	FPGA		Description	
Pin	Pin	Name	Net Name	Function
228	--	NC	Not connected	
229	--	NC	Not connected	
230	--	NC	Not connected	
231	--	NC	Not connected	
232	--	NC	Not connected	
233	--	NC	Not connected	
234	--	NC	Not connected	
235	--	NC	Not connected	
236	--	NC	Not connected	
237	--	GND	Ground	
238	--	GND		
239	--	+3.3v	+3.3v power supply	
240	--	+3.3v		

Connector U26-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
241	--	+3.3v	+3.3v power supply	
242	--	+3.3v		
243	--	GND	Ground	
244	--	GND		
245	Y15	BK4_IO_N6/**D0_C**	ARM_D00	uC data bus, data 0, only input to the FPGA. Only active when slave configuration mode is selected on M0-M1-M2
246	--	**M0**	ARM_GPIO9	Configuration Mode selection bit 0
247	W14	BK4_IO_P6/**D1**	ARM_D01	uC data bus, data 1
248	--	**M1**	ARM_GPIO10	Configuration Mode selection bit 1
249	Y14	BK4_IO_N3/**D2**	ARM_D02	uC data bus, data 2
250	--	**M2**	ARM_GPIO11	Configuration Mode selection bit 2
251	AA14	BK4_IO_P3/**D3**	ARM_D03	uC data bus, data 3
252	AD14	BK4_IO_P2/**DOUT**	ARM_#ACRESET	GPIO/DOUT during configuration
253	AC13	BK5_IO_N2/**D4**	ARM_D04	uC data bus, data 4
254	AC14	BK4_IO_N2/**INITB**	ARM_SYNC	GPIO/INITB during configuration
255	AB13	BK5_IO_P2/**D5**	ARM_D05	uC data bus, data 5
256	AC5	BK5_IO_N25/**RDWR_B**	ARM_BITCLK	GPIO/RDWR_B during configuration
257	AB12	BK5_IO_N5/**D6**	ARM_D06	uC data bus, data 6
258	AB5	BK5_IO_P25/**CS_B**	FPGA1_CS_B	GPIO/Chip select during configuration in slave parallel mode. Selectable from ARM_#CS2 or ARM_#PREG (R55, R56)
259	AA12	BK5_IO_P5/**D7**	ARM_D07	uC data bus, data 7
260	--	**PROG_B**	ARM_GPIO90	Resets FPGA configuration
261	AB10	BK5_IO_P11	ARM_D00	uC data bus, data 0
262	--	**CCLK**	FPGA1_CCLK	Configuration cock
263	AC10	BK5_IO_N11	ARM_D08	uC data bus, data 8
264	--	**DONE_G**	ARM_GPIO91	DONE_G configuration control line
265	W11	BK5_IO_P9	ARM_D09	uC data bus, data 9
266	AF5	BK5_IO_S10/VREF	ARM_D10	uC data bus, data 10
267	Y11	BK5_IO_N9	ARM_D11	uC data bus, data 11
268	AE6	BK5_IO_P20	ARM_D12	uC data bus, data 12
269	AD10	BK5_IO_S5	ARM_D13	uC data bus, data 13
270	AF6	BK5_IO_N20	ARM_D14	uC data bus, data 14
271	AC11	BK5_IO_S4	ARM_D15	uC data bus, data 15
272	AE7	BK5_IO_P18/VRN	ARM_D16	uC data bus, data 16
273	Y12	BK5_IO_N6/VREF	ARM_D17	uC data bus, data 17
274	AF7	BK5_IO_N18/VRP	ARM_D18	uC data bus, data 18
275	W12	BK5_IO_P6	ARM_D19	uC data bus, data 19
276	AE8	BK5_IO_P15	ARM_D20	uC data bus, data 20
277	AA11	BK5_IO_P8	ARM_D21	uC data bus, data 21
278	AF8	BK5_IO_N15	ARM_D22	uC data bus, data 22
279	AB11	BK5_IO_N8	ARM_D23	uC data bus, data 23
280	AE10	BK5_IO_P10*	ARM_D24	uC data bus, data 24
281	AA13	BK5_IO_S2	ARM_D25	uC data bus, data 25
282	AF10	BK5_IO_N10*	ARM_D26	uC data bus, data 26
283	AD13	BK5_IO_P1/CLK2	FPGA_2_FPGA40	FPGA bus, data 40
284	AE11	BK5_IO_P7*	ARM_D27	uC data bus, data 27
285	AE13	BK5_IO_N1/CLK3	ARM_L_PCLK	Pixel clock from ARM LCD controller

Connector U26-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
286	AF11	BK5_IO_N7*	ARM_D28	uC data bus, data 28
287	Y13	BK5_IO_N3	ARM_D29	uC data bus, data 29
288	AE12	BK5_IO_P4/VREF	ARM_D30	uC data bus, data 30
289	W13	BK5_IO_P3	ARM_D31	uC data bus, data 31
290	AF12	BK5_IO_N4	ARM_A00	uC address bus, bit 0
291	AD15	BK4_IO_S2	ARM_A01	uC address bus, bit 1
292	AF13	BK5_IO_S1/VREF	ARM_A02	uC address bus, bit 2
293	AE15	BK4_IO_N4	ARM_A03	uC address bus, bit 3
294	AE14	BK4_IO_N1/CLK1	ARM_SDCLK1	uC SDRAM controller clock
295	AF15	BK4_IO_P4	ARM_A04	uC address bus, bit 4
296	AF14	BK4_IO_P1/CLK0	FPGA_2_FPGA47	FPGA bus, data 47
297	--	GND	Ground	
298	--	GND		
299	--	VCC_5	+3.3V Power supply for FPGA IO bank 4 and bank 5	
300	--	VCC_5		
301	--	VCC_4		
302	--	VCC_4		
303	--	GND	Ground	
304	--	GND		
305	AB14	BK4_IO_S1/VREF	ARM_A05	uC address bus, bit 5
306	AD19	BK4_IO_S6*	ARM_A06	uC address bus, bit 6
307	AE16	BK4_IO_N7*	ARM_A07	uC address bus, bit 7
308	AF20	BK4_IO_P19	ARM_A08	uC address bus, bit 8
309	AF16	BK4_IO_P7/VREF*	ARM_A09	uC address bus, bit 9
310	AE20	BK4_IO_N19	ARM_A10	uC address bus, bit 10
311	AB18	BK4_IO_N14*	ARM_A11	uC address bus, bit 11
312	AF21	BK4_IO_S8	ARM_A12	uC address bus, bit 12
313	AC18	BK4_IO_P14*	ARM_A13	uC address bus, bit 13
314	AF22	BK4_IO_S9	ARM_A14	uC address bus, bit 14
315	AE19	BK4_IO_N16	ARM_A15	uC address bus, bit 15
316	AB16	BK4_IO_N8	ARM_A16	uC address bus, bit 16
317	AF19	BK4_IO_P16	ARM_A17	uC address bus, bit 17
318	AC16	BK4_IO_P8	ARM_A18	uC address bus, bit 18
319	AB15	BK4_IO_P5	ARM_#CS2	uC SRAM chip select 2
320	AD17	BK4_IO_N11/VREF	ARM_SDATA_OUT	uC serial data out AC97 interface
321	AA15	BK4_IO_N5	FPGA_2_FPGA39	FPGA bus, data 39
322	AB17	BK4_IO_P11	ARM_SDATA_IN_0	uC serial data input AC97 interface
323	Y16	BK4_IO_N9	ARM_#CS4	uC SRAM chip select 4
324	AF17	BK4_IO_P10*	ARM_IOIS16	uC memory interface IOIS16
325	AA16	BK4_IO_P9	ARM_#WE	uC memory interface #WE
326	AE17	BK4_IO_N10*	ARM_#OE	uC memory interface #OE
327	AC17	BK4_IO_N12	ARM_RD/#WR	uC memory interface RD/#WR
328	W15	BK4_IO_S3	ARM_RDY	uC memory interface RDY
329	AA17	BK4_IO_P12	FPGA_2_FPGA46	FPGA bus data 46
330	W16	BK4_IO_S4	FPGA_2_FPGA45	FPGA bus data 45
331	Y17	BK4_IO_S5/VREF	PX_CLK_Y4	output clock 4 from CDC706 PLL
332	AE18	BK4_IO_P13*	FPGA_2_FPGA44	FPGA bus data 44
333	AA18	BK4_IO_P15	ARM_#PWE	uC PCMCIA interface #PWE
334	AD18	BK4_IO_N13*	DVI_SCL	DVI subsystem I2C bus clock signals
335	Y18	BK4_IO_N15	ARM_#PCE1	uC PCMCIA interface #PCE1
336	AB19	BK4_IO_N17*	ARM_#PCE2	uC PCMCIA interface #PCE2
337	AA19	BK4_IO_P18*	ARM_#PIOW	uC PCMCIA interface #PIOW
338	AC19	BK4_IO_P17*	ARM_#PIOR	uC PCMCIA interface #PIOR
339	Y19	BK4_IO_N18*	PX_CLK_Y5	output clock 5 from CDC706 PLL
340	AC20	BK4_IO_P20	ARM_#POE	uC PCMCIA interface #POE
341	AA20	BK4_IO_S7	FPGA_2_FPGA41	FPGA bus data 41
342	AB20	BK4_IO_N20	FPGA_2_FPGA43	FPGA bus data 43
343	AC21	BK4_IO_P22	ARM_GPIO0	uC GPIO0
344	AE21	BK4_IO_P21	ARM_DREQ_0	uC DMA request signal
345	AB21	BK4_IO_N22	ARM_GPIO1	uC GPIO1
346	AD21	BK4_IO_N21	ARM_DVAL_0	uC DMA request signal
347	AE22	BK4_IO_P23	ARM_L_VSYNC	uC LCD controller vertical sync
348	AE23	BK4_IO_N24	FPGA_2_FPGA42	FPGA bus data 42
349	AD22	BK4_IO_N23/VREF	ARM_L_BIAS	uC LCD controller enable
350	AF23	BK4_IO_P24	ARM_L_DD0	uC LCD controller pixel data bit 0
351	AC22	BK4_IO_P26/VRN	ARM_L_CS	uC LCD controller select signal
352	AE24	BK4_IO_N25	ARM_L_DD1	uC LCD controller pixel data bit 1
353	AB22	BK4_IO_N26/VRP	ARM_L_LCLK	uC LCD controller line clock
354	AF24	BK4_IO_P25	ARM_L_DD2	uC LCD controller pixel data bit 2

Connector U26-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
355	AD25	BK4_IO_S11/VREF	ARM_L_FCLK	uC LCD controller frame clock
356	AD23	BK4_IO_S10	ARM_L_DD3	uC LCD controller pixel data bit 3
357	--	GND	Ground	
358	--	GND		
359	--	+3.3v	+3.3v power supply	
360	--	+3.3v		

Connector U26-D	FPGA		Description	
Pin	Pin	Name	Net Name	Function
361	--	+3.3v	+3.3v power supply	
362	--	+3.3v		
363	--	GND	Ground	
364	--	GND		
365	--	NC	Not connected	
366	--	NC	Not connected	
367	--	NC	Not connected	
368	--	NC	Not connected	
369	--	NC	Not connected	
370	--	NC	Not connected	
371	--	NC	Not connected	
372	--	NC	Not connected	
373	--	NC	Not connected	
374	--	NC	Not connected	
375	--	NC	Not connected	
376	--	NC	Not connected	
377	--	NC	Not connected	
378	--	NC	Not connected	
379	--	NC	Not connected	
380	--	NC	Not connected	
381	R2	BK6_IO_N5/VREF	ARM_L_DD4	uC LCD controller pixel data bit 4
382	--	NC	Not connected	
383	R1	BK6_IO_P5	ARM_L_DD5	uC LCD controller pixel data bit 5
384	--	NC	Not connected	
385	T1	BK6_IO_P9	ARM_L_DD6	uC LCD controller pixel data bit 6
386	P8	BK6_IO_N4	ARM_L_DD7	uC LCD controller pixel data bit 7
387	T2	BK6_IO_N9	ARM_L_DD8	uC LCD controller pixel data bit 8
388	P7	BK6_IO_P4	ARM_L_DD9	uC LCD controller pixel data bit 9
389	P6	BK6_IO_N3	ARM_L_DD10	uC LCD controller pixel data bit 10
390	T8	BK6_IO_N11	ARM_L_DD11	uC LCD controller pixel data bit 11
391	P5	BK6_IO_P3	ARM_L_DD12	uC LCD controller pixel data bit 12
392	T7	BK6_IO_P11	ARM_L_DD13	uC LCD controller pixel data bit 13
393	U3	BK6_IO_P13	ARM_L_DD14	uC LCD controller pixel data bit 14
394	T6	BK6_IO_N10	ARM_L_DD15	uC LCD controller pixel data bit 15
395	U4	BK6_IO_N13/VREF	ARM_L_DD16	uC LCD controller pixel data bit 16
396	T5	BK6_IO_P10	ARM_L_DD17	uC LCD controller pixel data bit 17
397	P1	BK6_IO_P1/VREF	FPGA_2_FPGA00	FPGA bus data 0
398	R6	BK6_IO_N7	FPGA_2_FPGA10	FPGA bus data 10
399	P2	BK6_IO_N1	FPGA_2_FPGA01	FPGA bus data 1
400	R5	BK6_IO_P7	FPGA_2_FPGA11	FPGA bus data 11
401	U7	BK6_IO_P17	FPGA_2_FPGA02	FPGA bus data 2
402	R8	BK6_IO_N8	FPGA_2_FPGA12	FPGA bus data 12
403	V7	BK6_IO_N17	FPGA_2_FPGA03	FPGA bus data 3
404	R7	BK6_IO_P8	FPGA_2_FPGA13	FPGA bus data 13
405	V6	BK6_IO_N20	FPGA_2_FPGA04	FPGA bus data 4
406	U5	BK6_IO_P14	FPGA_2_FPGA14	FPGA bus data 14
407	W5	BK6_IO_P20	FPGA_2_FPGA05	FPGA bus data 5
408	U6	BK6_IO_N14	ARM_SDA	uC I2C bus data line
409	W6	BK6_IO_P21	FPGA_2_FPGA06	FPGA bus data 6
410	R3	BK6_IO_P6	ARM_SCL	uC I2C bus clock line
411	W7	BK6_IO_N21	FPGA_2_FPGA07	FPGA bus data 7
412	T4	BK6_IO_N6	FPGA_2_FPGA15	FPGA bus data 15
413	Y6	BK6_IO_P26*	FPGA_2_FPGA08	FPGA bus data 8
414	P3	BK6_IO_P2	FPGA_2_FPGA16	FPGA bus data 16
415	Y7	BK6_IO_N26*	FPGA_2_FPGA09	FPGA bus data 9
416	P4	BK6_IO_N2	FPGA_2_FPGA17	FPGA bus data 17
417	--	GND	Ground	

Connector U26-D	FPGA		Description	
Pin	Pin	Name	Net Name	Function
418	--	GND		
419	--	VCC_7	+3.3v Power supply for FPGA IO bank 7	
420	--	VCC_7		
421	--	VCC_6	+3.3v Power supply for FPGA IO bank 6.	
422	--	VCC_6		
423	--	GND	Ground	
424	--	GND		
425	--	GND		
426	U2	BK6_IO_N12	FPGA_2_FPGA26	FPGA bus data 26
427	V5	BK6_IO_N16	FPGA_2_FPGA18	FPGA bus data 18
428	U1	BK6_IO_P12	FPGA_2_FPGA27	FPGA bus data 27
429	V4	BK6_IO_P16	FPGA_2_FPGA19	FPGA bus data 17
430	V3	BK6_IO_N15	FPGA_2_FPGA28	FPGA bus data 28
431	W4	BK6_IO_N19	FPGA_2_FPGA20	FPGA bus data 17
432	V2	BK6_IO_P15	FPGA_2_FPGA29	FPGA bus data 29
433	W3	BK6_IO_P19/VREF	FPGA_2_FPGA21	FPGA bus data 17
434	W1	BK6_IO_P18	FPGA_2_FPGA30	FPGA bus data 30
435	Y1	BK6_IO_P22*	FPGA_2_FPGA36	FPGA bus data 17
436	W2	BK6_IO_N18	FPGA_2_FPGA31	FPGA bus data 31
437	Y2	BK6_IO_N22*	FPGA_2_FPGA37	FPGA bus data 37
438	Y4	BK6_IO_P24*	FPGA_2_FPGA32	FPGA bus data 32
439	AA4	BK6_IO_N25*	FPGA_2_FPGA38	FPGA bus data 17
440	Y5	BK6_IO_N24*	RE1_A	Signal A from rotary encoder 1
441	AA3	BK6_IO_P25*	DVI_SDA	DVI I2C bus data line
442	AA1	BK6_IO_P23*	RE1_B	Signal B from rotary encoder 1
443	**AA5**	**BK6_IO_S1*****	**GND**	**Not present in XC3S1500**
444	AA2	BK6_IO_N23/VREF*	RE1_P	Push button signal from rotary encoder 1
445	AB3	BK6_IO_P29	RE2_A	Signal A from rotary encoder 2
446	AB1	BK6_IO_P27*	FPGA_2_FPGA33	FPGA bus data 33
447	AB4	BK6_IO_N29	RE2_B	Signal B from rotary encoder 2
448	AB2	BK6_IO_N27*	TRIG1_CMOS	output data signal from RS232 driver
449	AB6	BK5_IO_N23	RE2_P	Push button signal from rotary encoder 2
450	AC1	BK6_IO_P28	ACT1_CMOS	input data signal to R232 driver
451	AA6	BK5_IO_P23	FPGA_2_FPGA22	FPGA bus data 22
452	AC2	BK6_IO_N28/VREF	FPGA_2_FPGA34	FPGA bus data 34
453	AA7	BK5_IO_S9	FPGA_2_FPGA23	FPGA bus data 23
454	AD1	BK6_IO_P30/VRN	FPGA_2_FPGA35	FPGA bus data 35
455	AD4	BK5_IO_P24	FPGA_2_FPGA24	FPGA bus data 24
456	AD2	BK6_IO_N30/VRP	IO2_DB49	data line 49 of bus B for IO module 2
457	AE4	BK5_IO_N24	FPGA_2_FPGA25	FPGA bus data 25
458	AA8	BK5_IO_P17*	IO2_DB47	data line 47 of bus B for IO module 2
459	AD5	BK5_IO_P22	IO2_DB48	data line 48 of bus B for IO module 2
460	AB8	BK5_IO_N17/VREF*	IO2_DB45	data line 45 of bus B for IO module 2
461	AE5	BK5_IO_N22	IO2_DB46	data line 46 of bus B for IO module 2
462	Y8	BK5_IO_S8	IO2_DB43	data line 43 of bus B for IO module 2
463	AB7	BK5_IO_P19	IO2_DB44	data line 44 of bus B for IO module 2
464	AC9	BK5_IO_S6*	IO2_DB41	data line 41 of bus B for IO module 2
465	AC7	BK5_IO_N19	IO2_DB42	data line 42 of bus B for IO module 2
466	Y10	BK5_IO_P12/VREF	IO2_DB39	data line 39 of bus B for IO module 2
467	AD8	BK5_IO_N16*	IO2_DB40	data line 40 of bus B for IO module 2
468	AA10	BK5_IO_N12	IO2_DB37	data line 37 of bus B for IO module 2
469	AC8	BK5_IO_P16*	IO2_DB38	data line 38 of bus B for IO module 2
470	AA9	BK5_IO_N14	IO2_DB35	data line 35 of bus B for IO module 2
471	AD9	BK5_IO_P13*	IO2_DB36	data line 36 of bus B for IO module 2
472	Y9	BK5_IO_P14	IO2_DB33	data line 33 of bus B for IO module 2
473	AE9	BK5_IO_N13*	IO2_DB34	data line 34 of bus B for IO module 2
474	AC6	BK5_IO_P21	IO2_DB31	data line 31 of bus B for IO module 2
475	AB9	BK5_IO_S7	IO2_DB32	data line 32 of bus B for IO module 2
476	AD6	BK5_IO_N21	IO2_DB29	data line 29 of bus B for IO module 2
477	--	GND	Ground	
478	--	GND		
479	--	+3.3v	+3.3v power supply	
480	--	+3.3v		

3.2.2 FPGA 2 (U17)

The connectors U17-A, U17-B, U17-C and U17-D are SAMTEC QSH-060-02-L-D-A connected targeted for the ramDSP electronics ERIZOV0-XC3S1500 FPGA module. Next tables enumerate the pin assignment of the connectors for the FPGA module placed on position U17.

Connector U17-A	**FPGA**		**Description**	
Pin	Pin	Name	Net name	Function
1	--	+3.3v	+3.3v power supply	
2	--	+3.3v		
3	--	GND	Ground	
4	--	GND		
5	E5	BK0_IO_N25/VRP	IO4_DB48	data line 48 of bus B for IO module 4
6	B3	BK0_IO_S12/VREF	IO4_DB49	data line 49 of bus B for IO module 4
7	D5	BK0_IO_P25/VRN	IO4_DB46	data line 46 of bus B for IO module 4
8	A3	BK0_IO_S11	IO4_DB47	data line 47 of bus B for IO module 4
9	C5	BK0_IO_N23	IO4_DB44	data line 44 of bus B for IO module 4
10	C4	BK0_IO_S10	IO4_DB45	data line 45 of bus B for IO module 4
11	B5	BK0_IO_P23	IO4_DB42	data line 42 of bus B for IO module 4
12	A4	BK0_IO_P24/VREF	IO4_DB43	data line 43 of bus B for IO module 4
13	C6	BK0_IO_N21	IO4_DB40	data line 40 of bus B for IO module 4
14	B4	BK0_IO_N24	IO4_DB41	data line 41 of bus B for IO module 4
15	B6	BK0_IO_P21	IO4_DB38	data line 38 of bus B for IO module 4
16	A5	BK0_IO_S9	IO4_DB39	data line 39 of bus B for IO module 4
17	E7	BK0_IO_N20	IO4_DB36	data line 36 of bus B for IO module 4
18	C8	BK0_IO_S6*	IO4_DB37	data line 37 of bus B for IO module 4
19	D7	BK0_IO_P20	IO4_DB34	data line 34 of bus B for IO module 4
20	A6	BK0_IO_S8	IO4_DB35	data line 35 of bus B for IO module 4
21	E6	BK0_IO_N22	IO4_DB32	data line 32 of bus B for IO module 4
22	B7	BK0_IO_N19	IO4_DB33	data line 33 of bus B for IO module 4
23	D6	BK0_IO_P22	IO4_DB30	data line 30 of bus B for IO module 4
24	A7	BK0_IO_P19	IO4_DB31	data line 31 of bus B for IO module 4
25	F7	BK0_IO_S7/VREF	IO4_DB28	data line 28 of bus B for IO module 4
26	B8	BK0_IO_N16	IO4_DB29	data line 29 of bus B for IO module 4
27	E8	BK0_IO_N17*	IO4_DB26	data line 26 of bus B for IO module 4
28	A8	BK0_IO_P16	IO4_DB27	data line 27 of bus B for IO module 4
29	D8	BK0_IO_P17*	IO4_DB24	data line 24 of bus B for IO module 4
30	C12	BK0_IO_S2	IO4_DB25	data line 25 of bus B for IO module 4
31	G8	BK0_IO_N18*	IO4_DB22	data line 22 of bus B for IO module 4
32	B10	BK0_IO_N10*	IO4_DB23	data line 23 of bus B for IO module 4
33	F8	BK0_IO_P18*	IO4_DB20	data line 20 of bus B for IO module 4
34	A10	BK0_IO_P10*	IO4_DB21	data line 21 of bus B for IO module 4
35	E9	BK0_IO_N14*	IO4_DB18	data line 18 of bus B for IO module 4
36	B11	BK0_IO_N7*	IO4_DB19	data line 19 of bus B for IO module 4
37	D9	BK0_IO_P14*	IO4_DB16	data line 16 of bus B for IO module 4
38	A11	BK0_IO_P7/VREF*	IO4_DB17	data line 17 of bus B for IO module 4
39	C9	BK0_IO_N13*	IO4_DB14	data line 14 of bus B for IO module 4
40	B12	BK0_IO_N4	IO4_DB15	data line 15 of bus B for IO module 4
41	B9	BK0_IO_P13*	IO4_DB12	data line 12 of bus B for IO module 4
42	A12	BK0_IO_P4	IO4_DB13	data line 13 of bus B for IO module 4
43	G9	BK0_IO_N15	IO4_DB10	data line 10 of bus B for IO module 4
44	B13	BK0_IO_N1/CLK7	IO4_DB11	data line 11 of bus B for IO module 4
45	F9	BK0_IO_P15	IO4_DB08	data line 8 of bus B for IO module 4
46	A13	BK0_IO_P1/CLK6	IO4_DB09	data line 9 of bus B for IO module 4
47	G10	BK0_IO_S5/VREF	IO4_DB06	data line 6 of bus B for IO module 4
48	D11	BK0_IO_P8	IO4_DB07	data line 7 of bus B for IO module 4
49	F10	BK0_IO_N12	IO4_DB04	data line 4 of bus B for IO module 4
50	E11	BK0_IO_N8	IO4_DB05	data line 5 of bus B for IO module 4
51	E10	BK0_IO_P12	IO4_DB02	data line 2 of bus B for IO module 4
52	G11	BK0_IO_N9	IO4_DB03	data line 3 of bus B for IO module 4
53	D10	BK0_IO_N11	IO4_DB00	data line 0 of bus B for IO module 4
54	F11	BK0_IO_P9	IO4_DB01	data line 1 of bus B for IO module 4

Connector U17-A	FPGA		Description	
Pin	Pin	Name	Net name	Function
55	C10	BK0_IO_P11	IO3_DB47	data line 47 of bus B for IO module 3
56	H12	BK0_IO_S3	IO3_DB48	data line 48 of bus B for IO module 3
57	--	GND	Ground	
58	--	GND		
59	--	VCC_0	Power supply for FPGA IO bank 0 and bank 1	
60	--	VCC_0		
61	--	VCC_1		
62	--	VCC_1		
63	--	GND	Ground	
64	--	GND		
65	H11	BK0_IO_S4	IO3_DB45	data line 45 of bus B for IO module 3
66	E13	BK0_IO_S1	IO3_DB46	data line 46 of bus B for IO module 3
67	G12	BK0_IO_N6	IO3_DB43	data line 43 of bus B for IO module 3
68	C13	BK0_IO_P2/VREF	IO3_DB44	data line 44 of bus B for IO module 3
69	H13	BK0_IO_P6	IO3_DB41	data line 41 of bus B for IO module 3
70	D13	BK0_IO_N2	IO3_DB42	data line 42 of bus B for IO module 3
71	H14	BK1_IO_P3	IO3_DB39	data line 39 of bus B for IO module 3
72	C15	BK1_IO_S3/VREF	IO3_DB40	data line 40 of bus B for IO module 3
73	G14	BK1_IO_N3	IO3_DB37	data line 37 of bus B for IO module 3
74	A14	BK1_IO_S1	IO3_DB38	data line 38 of bus B for IO module 3
75	F12	BK0_IO_N5	IO3_DB35	data line 35 of bus B for IO module 3
76	B15	BK1_IO_P4	IO3_DB36	data line 36 of bus B for IO module 3
77	E12	BK0_IO_P5	IO3_DB33	data line 33 of bus B for IO module 3
78	A15	BK1_IO_N4	IO3_DB34	data line 34 of bus B for IO module 3
79	F13	BK0_IO_P3	IO3_DB31	data line 31 of bus B for IO module 3
80	B16	BK1_IO_P7*	IO3_DB32	data line 32 of bus B for IO module 3
81	G13	BK0_IO_N3	IO3_DB29	data line 29 of bus B for IO module 3
82	A16	BK1_IO_N7*	IO3_DB30	data line 30 of bus B for IO module 3
83	F14	BK1_IO_S2	IO3_DB27	data line 27 of bus B for IO module 3
84	B17	BK1_IO_P10*	IO3_DB28	data line 28 of bus B for IO module 3
85	D14	BK1_IO_N2/VREF	IO3_DB25	data line 25 of bus B for IO module 3
86	A17	BK1_IO_N10*	IO3_DB26	data line 26 of bus B for IO module 3
87	E14	BK1_IO_P2	IO3_DB23	data line 23 of bus B for IO module 3
88	C17	BK1_IO_S5/VREF	IO3_DB24	data line 24 of bus B for IO module 3
89	F15	BK1_IO_P5	IO3_DB21	data line 21 of bus B for IO module 3
90	B19	BK1_IO_P15	IO3_DB22	data line 22 of bus B for IO module 3
91	E15	BK1_IO_N5	IO3_DB19	data line 19 of bus B for IO module 3
92	A19	BK1_IO_N15	IO3_DB20	data line 20 of bus B for IO module 3
93	G16	BK1_IO_N9	IO3_DB17	data line 17 of bus B for IO module 3
94	B20	BK1_IO_P18	IO3_DB18	data line 18 of bus B for IO module 3
95	H16	BK1_IO_P9	IO3_DB15	data line 15 of bus B for IO module 3
96	A20	BK1_IO_N18/VREF	IO3_DB16	data line 16 of bus B for IO module 3
97	F17	BK1_IO_N12	IO3_DB13	data line 13 of bus B for IO module 3
98	B21	BK1_IO_P20	IO3_DB14	data line 14 of bus B for IO module 3
99	G17	BK1_IO_P12	IO3_DB11	data line 11 of bus B for IO module 3
100	A21	BK1_IO_N20	IO3_DB12	data line 12 of bus B for IO module 3
101	F18	BK1_IO_N14	IO3_DB09	data line 9 of bus B for IO module 3
102	A22	BK1_IO_S10	IO3_DB10	data line 10 of bus B for IO module 3
103	G18	BK1_IO_P14	IO3_DB07	data line 7 of bus B for IO module 3
104	D18	BK1_IO_S6/VREF*	IO3_DB08	data line 8 of bus B for IO module 3
105	F19	BK1_IO_P17*	IO3_DB05	data line 5 of bus B for IO module 3
106	A23	BK1_IO_S11	IO3_DB06	data line 6 of bus B for IO module 3
107	E19	BK1_IO_N17*	IO3_DB04	data line 4 of bus B for IO module 3
108	--	GND	Ground	
109	G19	BK1_IO_S8	IO3_DB03	data line 3 of bus B for IO module 3
110	--	TDI	TDI_FPGA1	JTAG data input
111	F20	BK1_IO_S9	IO3_DB02	data line 2 of bus B for IO module 3
112	--	TDO	TDO_FPGA1	JTAG data output
113	F21	BK1_IO_P23	IO3_DB01	data line 1 of bus B for IO module 3
114	--	TMS	TMS	JTAG chip select
115	E21	BK1_IO_N23	IO3_DB00	data line 0 of bus B for IO module 3
116	--	TCK	TCK	JTAG clock signal
117	--	GND	Ground	
118	--	GND		
119	--	+3.3v	+3.3v power supply	
120	--	+3.3v		

Connector U17-B	FPGA		Description	
Pin	Pin	Name	Net Name	Function
121	--	+3.3v	+3.3v power supply	
122	--	+3.3v		
123	--	GND	Ground	
124	--	GND		
125	C18	BK1_IO_P13*	FPGA_2_FPGA00	FPGA bus data 0
126	G15	BK1_IO_N6	FPGA_2_FPGA23	FPGA bus data 23
127	B18	BK1_IO_N13*	FPGA_2_FPGA01	FPGA bus data 1
128	H15	BK1_IO_P6	FPGA_2_FPGA24	FPGA bus data 24
129	D19	BK1_IO_P16*	FPGA_2_FPGA02	FPGA bus data 2
130	F16	BK1_IO_P8	FPGA_2_FPGA25	FPGA bus data 25
131	C19	BK1_IO_N16*	FPGA_2_FPGA03	FPGA bus data 3
132	E16	BK1_IO_N8	FPGA_2_FPGA26	FPGA bus data 26
133	D20	BK1_IO_N19	FPGA_2_FPGA04	FPGA bus data 4
134	D16	BK1_IO_S4	FPGA_2_FPGA27	FPGA bus data 27
135	E20	BK1_IO_P19	FPGA_2_FPGA05	FPGA bus data 5
136	D17	BK1_IO_N11	FPGA_2_FPGA28	FPGA bus data 28
137	C21	BK1_IO_N21	FPGA_2_FPGA06	FPGA bus data 6
138	E17	BK1_IO_P11	FPGA_2_FPGA29	FPGA bus data 29
139	D21	BK1_IO_P21	FPGA_2_FPGA07	FPGA bus data 7
140	E18	BK1_IO_S7	FPGA_2_FPGA30	FPGA bus data 30
141	B22	BK1_IO_N22/VREF	FPGA_2_FPGA08	FPGA bus data 8
142	C25	BK2_IO_N1/VRP	FPGA_2_FPGA31	FPGA bus data 31
143	C22	BK1_IO_P22	FPGA_2_FPGA09	FPGA bus data 9
144	C26	BK2_IO_P1/VRN	FPGA_2_FPGA32	FPGA bus data 32
145	B23	BK1_IO_N24	FPGA_2_FPGA10	FPGA bus data 10
146	D25	BK2_IO_N3/VREF	FPGA_2_FPGA33	FPGA bus data 33
147	C23	BK1_IO_P24	FPGA_2_FPGA11	FPGA bus data 11
148	D26	BK2_IO_P3	FPGA_2_FPGA34	FPGA bus data 34
149	D22	BK1_IO_N25/VRP	FPGA_2_FPGA12	FPGA bus data 12
150	E25	BK2_IO_N4*	FPGA_2_FPGA35	FPGA bus data 35
151	E22	BK1_IO_P25/VRN	FPGA_2_FPGA13	FPGA bus data 13
152	E26	BK2_IO_P4*	FPGA_2_FPGA36	FPGA bus data 36
153	E23	BK2_IO_N2	FPGA_2_FPGA14	FPGA bus data 14
154	F25	BK2_IO_N8/VREF*	FPGA_2_FPGA37	FPGA bus data 37
155	E24	BK2_IO_P2	FPGA_2_FPGA15	FPGA bus data 15
156	F26	BK2_IO_P8*	FPGA_2_FPGA38	FPGA bus data 38
157	F23	BK2_IO_N6*	FPGA_2_FPGA16	FPGA bus data 16
158	G25	BK2_IO_N9*	FPGA_2_FPGA39	FPGA bus data 39
159	F24	BK2_IO_P6*	FPGA_2_FPGA17	FPGA bus data 17
160	G26	BK2_IO_P9*	FPGA_2_FPGA40	FPGA bus data 40
161	K20	BK2_IO_P14	FPGA_2_FPGA18	FPGA bus data 18
162	H25	BK2_IO_N13	FPGA_2_FPGA41	FPGA bus data 41
163	J20	BK2_IO_N14	FPGA_2_FPGA19	FPGA bus data 19
164	H26	BK2_IO_P13	FPGA_2_FPGA42	FPGA bus data 42
165	J22	BK2_IO_N15	FPGA_2_FPGA20	FPGA bus data 20
166	K25	BK2_IO_N19	FPGA_2_FPGA43	FPGA bus data 43
167	J23	BK2_IO_P15	FPGA_2_FPGA21	FPGA bus data 21
168	K26	BK2_IO_P19	FPGA_2_FPGA44	FPGA bus data 44
169	K21	BK2_IO_N17/VREF	FPGA_2_FPGA22	FPGA bus data 22
170	L25	BK2_IO_N22	FPGA_2_FPGA45	FPGA bus data 45
171	K22	BK2_IO_P17	DVI_OUT_VSYNC	Vertical Sync for DVI out
172	L26	BK2_IO_P22	FPGA_2_FPGA46	FPGA bus data 46
173	L21	BK2_IO_N21	DVI_OUT_HSYNC	Horizontal Sync for DVI out
174	M25	BK2_IO_N26/VREF	DVI_OUT_#RST	Reset for DVI out
175	L22	BK2_IO_P21	DVI_OUT_DE	Data enable for DVI out
176	M26	BK2_IO_P26	DVI_OUT_MSEN/PO1	MSEN/PO1 for DVI out
177	--	GND	Ground	
178	--	GND		
179	--	VCC_2	+3.3V power supply applied to bank 2	
180	--	VCC_2		
181	--	VCC_3	+3.3V power supply applied to bank 3	
182	--	VCC_3		
183	--	GND	Ground	
184	--	GND		
185	N22	BK2_IO_P28	FPGA_DVI_OUT_DCK+	Clock signal for DVI out
186	N25	BK2_IO_N30	FPGA_DVI_OUT_DATA16	DVI out Data bus bit 16
187	N21	BK2_IO_N28	FPGA_DVI_OUT_DATA23	DVI out Data bus bit 23
188	N26	BK2_IO_P30/VREF	FPGA_DVI_OUT_DATA22	DVI out Data bus bit 22
189	K24	BK2_IO_P18	FPGA_DVI_OUT_DATA21	DVI out Data bus bit 21

Connector U17-B	FPGA		Description	
Pin	Pin	Name	Net Name	Function
190	G20	BK2_IO_N5*	FPGA_DVI_OUT_DATA20	DVI out Data bus bit 20
191	K23	BK2_IO_N18	FPGA_DVI_OUT_DATA19	DVI out Data bus bit 19
192	G21	BK2_IO_P5*	FPGA_DVI_OUT_DATA18	DVI out Data bus bit 18
193	M19	BK2_IO_N23	FPGA_DVI_OUT_DATA17	DVI out Data bus bit 17
194	**F22**	**BK2_IO_S1****	**GND**	**Not present in XC3S1500**
195	M20	BK2_IO_P23	FPGA_DVI_OUT_DATA15	DVI out Data bus bit 15
196	H20	BK2_IO_N10	FPGA_DVI_OUT_DATA14	DVI out Data bus bit 14
197	N20	BK2_IO_P27	FPGA_DVI_OUT_DATA13	DVI out Data bus bit 13
198	H21	BK2_IO_P10	FPGA_DVI_OUT_DATA12	DVI out Data bus bit 12
199	N19	BK2_IO_N27	FPGA_DVI_OUT_DATA11	DVI out Data bus bit 11
200	J21	BK2_IO_P11	FPGA_DVI_OUT_DATA10	DVI out Data bus bit 10
201	M22	BK2_IO_P24	FPGA_DVI_OUT_DATA09	DVI out Data bus bit 9
202	H22	BK2_IO_N11	FPGA_DVI_OUT_DATA08	DVI out Data bus bit 8
203	M21	BK2_IO_N24	FPGA_DVI_OUT_DATA07	DVI out Data bus bit 7
204	G22	BK2_IO_N7*	FPGA_DVI_OUT_DATA06	DVI out Data bus bit 6
205	L20	BK2_IO_P20	FPGA_DVI_OUT_DATA05	DVI out Data bus bit 5
206	G23	BK2_IO_P7*	FPGA_DVI_OUT_DATA04	DVI out Data bus bit 4
207	L19	BK2_IO_N20	FPGA_DVI_OUT_DATA03	DVI out Data bus bit 3
208	H24	BK2_IO_P12/VREF	FPGA_DVI_OUT_DATA02	DVI out Data bus bit 2
209	--	NC	Not connected	
210	H23	BK2_IO_N12	FPGA_DVI_OUT_DATA01	DVI out Data bus bit 1
211	--	NC	Not connected	
212	J24	BK2_IO_N16	FPGA_DVI_OUT_DATA00	DVI out Data bus bit 0
213	--	NC	Not connected	
214	J25	BK2_IO_P16	AN_OUT_SYNCT	SYNCT for analog RGB output
215	--	NC	Not connected	
216	M24	BK2_IO_P25	AN_OUT_#BLANK	#BLANK for analog RGB output
217	--	NC	Not connected	
218	L23	BK2_IO_N25	AN_OUT_SYNC	SYNC for analog RGB output
219	--	NC	Not connected	
220	N24	BK2_IO_P29	AN_OUT_M2	M2 for analog RGB output
221	--	NC	Not connected	
222	N23	BK2_IO_N29	AN_OUT_M1	M1 for analog RGB output
223	--	NC	Not connected	
224	--	NC	Not connected	
225	--	NC	Not connected	
226	--	NC	Not connected	
227	--	NC	Not connected	
228	--	NC	Not connected	
229	--	NC	Not connected	
230	--	NC	Not connected	
231	--	NC	Not connected	
232	--	NC	Not connected	
233	--	NC	Not connected	
234	--	NC	Not connected	
235	--	NC	Not connected	
236	--	NC	Not connected	
237	--	GND	Ground	
238	--	GND		
239	--	+3.3v	+3.3v power supply	
240	--	+3.3v		

Connector U17-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
241	--	+3.3v	+3.3v power supply	
242	--	+3.3v		
243	--	GND	Ground	
244	--	GND		
245	Y15	BK4_IO_N6/**D0_C**	ARM_D00	uC data bus, data 0, only input to the FPGA. Only active when slave configuration mode is selected on M0-M1-M2
246	--	**M0**	ARM_GPIO9	Configuration Mode selection bit 0
247	W14	BK4_IO_P6/**D1**	ARM_D01	uC data bus, data 1
248	--	**M1**	ARM_GPIO10	Configuration Mode selection bit 1
249	Y14	BK4_IO_N3/**D2**	ARM_D02	uC data bus, data 2

Connector U17-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
250	--	**M2**	ARM_GPIO11	Configuration Mode selection bit 2
251	AA14	BK4_IO_P3/**D3**	ARM_D03	uC data bus, data 3
252	AD14	BK4_IO_P2/**DOUT**	ARM_GPIO1	GPIO/DOUT during configuration
253	AC13	BK5_IO_N2/**D4**	ARM_D04	uC data bus, data 4
254	AC14	BK4_IO_N2/**INITB**	#INIT_FPGA_2	GPIO/INITB during configuration
255	AB13	BK5_IO_P2/**D5**	ARM_D05	uC data bus, data 5
256	AC5	BK5_IO_N25/**RDWR_B**	RD/#WR_FPGA_2	GPIO/RDWR_B during configuration
257	AB12	BK5_IO_N5/**D6**	ARM_D06	uC data bus, data 6
258	AB5	BK5_IO_P25/**CS_B**	FPGA2_CS_B	GPIO/Chip select during configuration in slave parallel mode. Selectable from ARM_#CS2 or ARM_#PREG (R55, R56)
259	AA12	BK5_IO_P5/**D7**	ARM_D07	uC data bus, data 7
260	--	**PROG_B**	#PROG_FPGA_2	Resets FPGA configuration
261	AB10	BK5_IO_P11	ARM_D00	uC data bus, data 0
262	--	**CCLK**	FPGA2_CCLK	Configuration cock
263	AC10	BK5_IO_N11	ARM_D08	uC data bus, data 8
264	--	**DONE_G**	DONE_FPGA_2	DONE_G configuration control line
265	W11	BK5_IO_P9	ARM_D09	uC data bus, data 9
266	AF5	BK5_IO_S10/VREF	ARM_D10	uC data bus, data 10
267	Y11	BK5_IO_N9	ARM_D11	uC data bus, data 11
268	AE6	BK5_IO_P20	ARM_D12	uC data bus, data 12
269	AD10	BK5_IO_S5	ARM_D13	uC data bus, data 13
270	AF6	BK5_IO_N20	ARM_D14	uC data bus, data 14
271	AC11	BK5_IO_S4	ARM_D15	uC data bus, data 15
272	AE7	BK5_IO_P18/VRN	ARM_D16	uC data bus, data 16
273	Y12	BK5_IO_N6/VREF	ARM_D17	uC data bus, data 17
274	AF7	BK5_IO_N18/VRP	ARM_D18	uC data bus, data 18
275	W12	BK5_IO_P6	ARM_D19	uC data bus, data 19
276	AE8	BK5_IO_P15	ARM_D20	uC data bus, data 20
277	AA11	BK5_IO_P8	ARM_D21	uC data bus, data 21
278	AF8	BK5_IO_N15	ARM_D22	uC data bus, data 22
279	AB11	BK5_IO_N8	ARM_D23	uC data bus, data 23
280	AE10	BK5_IO_P10*	ARM_D24	uC data bus, data 24
281	AA13	BK5_IO_S2	ARM_D25	uC data bus, data 25
282	AF10	BK5_IO_N10*	ARM_D26	uC data bus, data 26
283	AD13	BK5_IO_P1/CLK2	PX_CLK_Y2	output clock 2 from CDC706 PLL
284	AE11	BK5_IO_P7*	ARM_D27	uC data bus, data 27
285	AE13	BK5_IO_N1/CLK3	PX_CLK_Y3	output clock 3 from CDC706 PLL
286	AF11	BK5_IO_N7*	ARM_D28	uC data bus, data 28
287	Y13	BK5_IO_N3	ARM_D29	uC data bus, data 29
288	AE12	BK5_IO_P4/VREF	ARM_D30	uC data bus, data 30
289	W13	BK5_IO_P3	ARM_D31	uC data bus, data 31
290	AF12	BK5_IO_N4	ARM_A00	uC address bus, bit 0
291	AD15	BK4_IO_S2	ARM_A01	uC address bus, bit 1
292	AF13	BK5_IO_S1/VREF	ARM_A02	uC address bus, bit 2
293	AE15	BK4_IO_N4	ARM_A03	uC address bus, bit 3
294	AE14	BK4_IO_N1/CLK1	ARM_SDCLK1	uC SDRAM controller clock
295	AF15	BK4_IO_P4	ARM_A04	uC address bus, bit 4
296	AF14	BK4_IO_P1/CLK0	FPGA_2_FPGA47	FPGA bus, data 47
297	--	GND	Ground	
298	--	GND		
299	--	VCC_5	+3.3V Power supply for FPGA IO bank 4 and bank 5	
300	--	VCC_5		
301	--	VCC_4		
302	--	VCC_4		
303	--	GND	Ground	
304	--	GND		
305	AB14	BK4_IO_S1/VREF	ARM_A05	uC address bus, bit 5
306	AD19	BK4_IO_S6*	ARM_A06	uC address bus, bit 6
307	AE16	BK4_IO_N7*	ARM_A07	uC address bus, bit 7
308	AF20	BK4_IO_P19	ARM_A08	uC address bus, bit 8
309	AF16	BK4_IO_P7/VREF*	ARM_A09	uC address bus, bit 9
310	AE20	BK4_IO_N19	ARM_A10	uC address bus, bit 10
311	AB18	BK4_IO_N14*	ARM_A11	uC address bus, bit 11
312	AF21	BK4_IO_S8	ARM_A12	uC address bus, bit 12
313	AC18	BK4_IO_P14*	ARM_A13	uC address bus, bit 13
314	AF22	BK4_IO_S9	ARM_A14	uC address bus, bit 14
315	AE19	BK4_IO_N16	ARM_A15	uC address bus, bit 15

Connector U17-C	FPGA		Description	
Pin	Pin	Name	Net Name	Function
316	AB16	BK4_IO_N8	ARM_A16	uC address bus, bit 16
317	AF19	BK4_IO_P16	ARM_A17	uC address bus, bit 17
318	AC16	BK4_IO_P8	ARM_A18	uC address bus, bit 18
319	AB15	BK4_IO_P5	ARM_#CS2	uC SRAM chip select 2
320	AD17	BK4_IO_N11/VREF	FPGA_GY0	Analog output, green bit 0
321	AA15	BK4_IO_N5	IO3_DB49	data line 49 of bus B for IO module 3
322	AB17	BK4_IO_P11	FPGA_GY1	Analog output, green bit 1
323	Y16	BK4_IO_N9	ARM_#CS4	uC SRAM chip select 4
324	AF17	BK4_IO_P10*	FPGA_GY2	Analog output, green bit 2
325	AA16	BK4_IO_P9	ARM_#WE	uC memory interface #WE
326	AE17	BK4_IO_N10*	FPGA_GY3	Analog output, green bit 3
327	AC17	BK4_IO_N12	ARM_#OE	uC memory interface #OE
328	W15	BK4_IO_S3	FPGA_GY4	Analog output, green bit 4
329	AA17	BK4_IO_P12	FPGA_GY7	Analog output, green bit 7
330	W16	BK4_IO_S4	FPGA_GY5	Analog output, green bit 5
331	Y17	BK4_IO_S5/VREF	FPGA_GY8	Analog output, green bit 8
332	AE18	BK4_IO_P13*	FPGA_GY6	Analog output, green bit 6
333	AA18	BK4_IO_P15	FPGA_GY9	Analog output, green bit 9
334	AD18	BK4_IO_N13*	FPGA_RPR0	Analog output, red bit 0
335	Y18	BK4_IO_N15	FPGA_RPR2	Analog output, red bit 2
336	AB19	BK4_IO_N17*	FPGA_RPR1	Analog output, red bit 1
337	AA19	BK4_IO_P18*	FPGA_RPR4	Analog output, red bit 4
338	AC19	BK4_IO_P17*	FPGA_RPR3	Analog output, red bit 3
339	Y19	BK4_IO_N18*	FPGA_RPR6	Analog output, red bit 6
340	AC20	BK4_IO_P20	FPGA_RPR5	Analog output, red bit 5
341	AA20	BK4_IO_S7	FPGA_RPR8	Analog output, red bit 8
342	AB20	BK4_IO_N20	FPGA_RPR7	Analog output, red bit 7
343	AC21	BK4_IO_P22	FPGA_BPB0	Analog output, blue bit 0
344	AE21	BK4_IO_P21	FPGA_RPR9	Analog output, red bit 9
345	AB21	BK4_IO_N22	FPGA_BPB2	Analog output, blue bit 2
346	AD21	BK4_IO_N21	FPGA_BPB1	Analog output, blue bit 1
347	AE22	BK4_IO_P23	FPGA_BPB4	Analog output, blue bit 4
348	AE23	BK4_IO_N24	FPGA_BPB3	Analog output, blue bit 3
349	AD22	BK4_IO_N23/VREF	FPGA_BPB6	Analog output, blue bit 6
350	AF23	BK4_IO_P24	FPGA_BPB5	Analog output, blue bit 5
351	AC22	BK4_IO_P26/VRN	FPGA_BPB8	Analog output, blue bit 8
352	AE24	BK4_IO_N25	FPGA_BPB7	Analog output, blue bit 7
353	AB22	BK4_IO_N26/VRP	ANALOG_OUT_HSYNC	Analog output, horizontal sync
354	AF24	BK4_IO_P25	FPGA_BPB9	Analog output, blue bit 9
355	AD25	BK4_IO_S11/VREF	ANALOG_OUT_VSYNC	Analog output, vertical sync
356	AD23	BK4_IO_S10	FPGA_AN_OUT_PCLK	Pixel clock for analog output
357	--	GND	Ground	
358	--	GND		
359	--	+3.3v	+3.3v power supply	
360	--	+3.3v		

Connector U17-D	FPGA		Description	
Pin	Pin	Name	Net Name	Function
361	--	+3.3v	+3.3v power supply	
362	--	+3.3v		
363	--	GND	Ground	
364	--	GND		
365	--	NC	Not connected	
366	--	NC	Not connected	
367	--	NC	Not connected	
368	--	NC	Not connected	
369	--	NC	Not connected	
370	--	NC	Not connected	
371	--	NC	Not connected	
372	--	NC	Not connected	
373	--	NC	Not connected	
374	--	NC	Not connected	
375	--	NC	Not connected	
376	--	NC	Not connected	
377	--	NC	Not connected	
378	--	NC	Not connected	

Connector U17-D	FPGA		Description	
Pin	Pin	Name	Net Name	Function
379	--	NC	Not connected	
380	--	NC	Not connected	
381	R2	BK6_IO_N5/VREF	N.C.	N.C.
382	--	NC	Not connected	
383	R1	BK6_IO_P5	VIDEO_AN15	Analog video input, bit 15
384	--	NC	Not connected	
385	T1	BK6_IO_P9	VIDEO_AN13	Analog video input, bit 13
386	P8	BK6_IO_N4	VIDEO_AN14	Analog video input, bit 14
387	T2	BK6_IO_N9	VIDEO_AN11	Analog video input, bit 11
388	P7	BK6_IO_P4	VIDEO_AN12	Analog video input, bit 12
389	P6	BK6_IO_N3	VIDEO_AN09	Analog video input, bit 9
390	T8	BK6_IO_N11	VIDEO_AN10	Analog video input, bit 10
391	P5	BK6_IO_P3	VIDEO_AN07	Analog video input, bit 7
392	T7	BK6_IO_P11	VIDEO_AN08	Analog video input, bit 8
393	U3	BK6_IO_P13	VIDEO_AN05	Analog video input, bit 5
394	T6	BK6_IO_N10	VIDEO_AN06	Analog video input, bit 6
395	U4	BK6_IO_N13/VREF	VIDEO_AN03	Analog video input, bit 3
396	T5	BK6_IO_P10	VIDEO_AN04	Analog video input, bit 4
397	P1	BK6_IO_P1/VREF	VIDEO_AN01	Analog video input, bit 1
398	R6	BK6_IO_N7	VIDEO_AN02	Analog video input, bit 2
399	P2	BK6_IO_N1	VIDEO_AN_FIELD	Analog video input, field signal
400	R5	BK6_IO_P7	VIDEO_AN00	Analog video input, bit 0
401	U7	BK6_IO_P17	VIDEO_AN_VS	Analog video input vertical sync
402	R8	BK6_IO_N8	VIDEO_AN_LLC	Analog video input PLL signal
403	V7	BK6_IO_N17	VIDEO_AN_HS	Analog video input horizontal sync
404	R7	BK6_IO_P8	VIDEO_AN_SFL	Analog video input SFL
405	V6	BK6_IO_N20	VIDEO_AN_#INTRQ	Analog video input interrupt request
406	U5	BK6_IO_P14	VIDEO_AN_#RESET	Analog video input reset signal
407	W5	BK6_IO_P20	DVI_IN_OPTIONS	Selectable control signal from DVI input interface
408	U6	BK6_IO_N14	VIDEO_AN_#PWRDWN	Analog video input power down signal
409	W6	BK6_IO_P21	DVI_IN_CTL2	DVI input, Control signal 2
410	R3	BK6_IO_P6	DVI_SCL	DVI subsystem I2C clock signal
411	W7	BK6_IO_N21	DVI_IN_CTL1	DVI input, Control signal 1
412	T4	BK6_IO_N6	DVI_SDA	DVI subsystem I2C data signal
413	Y6	BK6_IO_P26*	DVI_IN_CTL0	DVI input, Control signal 0
414	P3	BK6_IO_P2	DVI_IN_DE	DVI input data enable
415	Y7	BK6_IO_N26*	DVI_IN_HSOUT	DVI input, horizontal sync
416	P4	BK6_IO_N2	DVI_IN_VSOUT	DVI input vertical sync
417	--	GND	Ground	
418	--	GND		
419	--	VCC_7	+3.3v Power supply for FPGA IO bank 7	
420	--	VCC_7		
421	--	VCC_6	+3.3v Power supply for FPGA IO bank 6.	
422	--	VCC_6		
423	--	GND	Ground	
424	--	GND		
425	--	GND		
426	U2	BK6_IO_N12	DVI_IN_BLUE_A0	DVI input channel A, blue bit 0
427	V5	BK6_IO_N16	DVI_IN_SOGOUT	DVI input sync on green output
428	U1	BK6_IO_P12	DVI_IN_DATACK	DVI input data acknowledge
429	V4	BK6_IO_P16	DVI_IN_BLUE_B6	DVI input channel B, blue bit 6
430	V3	BK6_IO_N15	DVI_IN_BLUE_B7	DVI input channel B, blue bit 7
431	W4	BK6_IO_N19	DVI_IN_BLUE_B4	DVI input channel B, blue bit 4
432	V2	BK6_IO_P15	DVI_IN_BLUE_B5	DVI input channel B, blue bit 5
433	W3	BK6_IO_P19/VREF	DVI_IN_BLUE_B2	DVI input channel B, blue bit 2
434	W1	BK6_IO_P18	DVI_IN_BLUE_B3	DVI input channel B, blue bit 3
435	Y1	BK6_IO_P22*	DVI_IN_BLUE_B0	DVI input channel B, blue bit 0
436	W2	BK6_IO_N18	DVI_IN_BLUE_B1	DVI input channel B, blue bit 1
437	Y2	BK6_IO_N22*	DVI_IN_BLUE_A6	DVI input channel A, blue bit 6
438	Y4	BK6_IO_P24*	DVI_IN_BLUE_A7	DVI input channel A, blue bit 7
439	AA4	BK6_IO_N25*	DVI_IN_BLUE_A4	DVI input channel A, blue bit 4
440	Y5	BK6_IO_N24*	DVI_IN_BLUE_A5	DVI input channel A, blue bit 5
441	AA3	BK6_IO_P25*	DVI_IN_BLUE_A2	DVI input channel A, blue bit 2
442	AA1	BK6_IO_P23*	DVI_IN_BLUE_A3	DVI input channel A, blue bit 3
443	**AA5**	**BK6_IO_S1*** **	**GND**	**Not present in XC3S1500**
444	AA2	BK6_IO_N23/VREF*	DVI_IN_BLUE_A1	DVI input channel A, blue bit 1
445	AB3	BK6_IO_P29	DVI_IN_GREEN_B6	DVI input channel B, green bit 6
446	AB1	BK6_IO_P27*	DVI_IN_GREEN_B7	DVI input channel B, green bit 7

Connector U17-D	FPGA		Description	
Pin	Pin	Name	Net Name	Function
447	AB4	BK6_IO_N29	DVI_IN_GREEN_B4	DVI input channel B, green bit 4
448	AB2	BK6_IO_N27*	DVI_IN_GREEN_B5	DVI input channel B, green bit 5
449	AB6	BK5_IO_N23	DVI_IN_GREEN_B2	DVI input channel B, green bit 2
450	AC1	BK6_IO_P28	DVI_IN_GREEN_B3	DVI input channel B, green bit 3
451	AA6	BK5_IO_P23	DVI_IN_GREEN_B0	DVI input channel B, green bit 0
452	AC2	BK6_IO_N28/VREF	DVI_IN_GREEN_B1	DVI input channel B, green bit 1
453	AA7	BK5_IO_S9	DVI_IN_GREEN_A6	DVI input channel A, green bit 6
454	AD1	BK6_IO_P30/VRN	DVI_IN_GREEN_A7	DVI input channel A, green bit 7
455	AD4	BK5_IO_P24	DVI_IN_GREEN_A4	DVI input channel A, green bit 4
456	AD2	BK6_IO_N30/VRP	DVI_IN_GREEN_A5	DVI input channel A, green bit 5
457	AE4	BK5_IO_N24	DVI_IN_GREEN_A2	DVI input channel A, green bit 2
458	AA8	BK5_IO_P17*	DVI_IN_GREEN_A3	DVI input channel A, green bit 3
459	AD5	BK5_IO_P22	DVI_IN_GREEN_A0	DVI input channel A, green bit 0
460	AB8	BK5_IO_N17/VREF*	DVI_IN_GREEN_A1	DVI input channel A, green bit 1
461	AE5	BK5_IO_N22	DVI_IN_RED_B6	DVI input channel B, red bit 6
462	Y8	BK5_IO_S8	DVI_IN_RED_B7	DVI input channel B, red bit 7
463	AB7	BK5_IO_P19	DVI_IN_RED_B4	DVI input channel B, red bit 4
464	AC9	BK5_IO_S6*	DVI_IN_RED_B5	DVI input channel B, red bit 5
465	AC7	BK5_IO_N19	DVI_IN_RED_B2	DVI input channel B, red bit 2
466	Y10	BK5_IO_P12/VREF	DVI_IN_RED_B3	DVI input channel B, red bit 3
467	AD8	BK5_IO_N16*	DVI_IN_RED_B0	DVI input channel B, red bit 0
468	AA10	BK5_IO_N12	DVI_IN_RED_B1	DVI input channel B, red bit 1
469	AC8	BK5_IO_P16*	DVI_IN_RED_A6	DVI input channel A, red bit 6
470	AA9	BK5_IO_N14	DVI_IN_RED_A7	DVI input channel A, red bit 7
471	AD9	BK5_IO_P13*	DVI_IN_RED_A4	DVI input channel A, red bit 4
472	Y9	BK5_IO_P14	DVI_IN_RED_A5	DVI input channel A, red bit 5
473	AE9	BK5_IO_N13*	DVI_IN_RED_A2	DVI input channel A, red bit 2
474	AC6	BK5_IO_P21	DVI_IN_RED_A3	DVI input channel A, red bit 3
475	AB9	BK5_IO_S7	DVI_IN_RED_A0	DVI input channel A, red bit 0
476	AD6	BK5_IO_N21	DVI_IN_RED_A1	DVI input channel A, red bit 1
477	--	GND	Ground	
478	--	GND		
479	--	+3.3v	+3.3v power supply	
480	--	+3.3v		

3.2.3 FPGA module Top connectors

Every FPGA module is stackable using two connectors (JT1 and JT2) located on its top layer. The connectors JT1 and JT2 located on the top layer are high speed SAMTEC QSH-060-02-L-D-A connectors that mate to SAMTEC QTH-060-02-L-D-A.

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
1	--	+3.3v	+3.3v power supply	
2	--	+3.3v		
3	--	GND	Ground	
4	--	GND		
5	F5	BK7_IO_N30/VRP	T.B.D.	GPIO/Bank 7 VRP
6	H5	BK7_IO_P20/VREF	T.B.D.	GPIO/Bank 7 VREF
7	F6	BK7_IO_P30/VRN	T.B.D.	GPIO/Bank 7 VRN
8	J6	BK7_IO_N20	T.B.D.	GPIO
9	G6	BK7_IO_N27*	T.B.D.	GPIO
10	J5	BK7_IO_P16	T.B.D.	GPIO
11	G7	BK7_IO_P27*	T.B.D.	GPIO
12	J4	BK7_IO_N16	T.B.D.	GPIO
13	H6	BK7_IO_N22*	T.B.D.	GPIO
14	M7	BK7_IO_N8	T.B.D.	GPIO
15	H7	BK7_IO_P22/VREF*	T.B.D.	GPIO/Bank 7 VREF

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
16	M8	BK7_IO_P8	T.B.D.	GPIO
17	N5	BK7_IO_N3	T.B.D.	GPIO
18	M6	BK7_IO_N7	T.B.D.	GPIO
19	N6	BK7_IO_P3	T.B.D.	GPIO
20	M5	BK7_IO_P7	T.B.D.	GPIO
21	F4	BK7_IO_P25*	T.B.D.	GPIO
22	D2	BK7_IO_P28	T.B.D.	GPIO
23	F3	BK7_IO_N25*	T.B.D.	GPIO
24	D1	BK7_IO_N28/VREF	T.B.D.	GPIO/Bank 7 VREF
25	G5	BK7_IO_P24*	T.B.D.	GPIO
26	E2	BK7_IO_P26*	T.B.D.	GPIO
27	G4	BK7_IO_N24*	T.B.D.	GPIO
28	E1	BK7_IO_N26*	T.B.D.	GPIO
29	L4	BK7_IO_P6	T.B.D.	GPIO
30	F2	BK7_IO_P23*	T.B.D.	GPIO
31	M3	BK7_IO_N6	T.B.D.	GPIO
32	F1	BK7_IO_N23*	T.B.D.	GPIO
33	H3	BK7_IO_N19	T.B.D.	GPIO
34	G2	BK7_IO_P21	T.B.D.	GPIO
35	H4	BK7_IO_P19	T.B.D.	GPIO
36	G1	BK7_IO_N21	T.B.D.	GPIO
37	J3	BK7_IO_P15	T.B.D.	GPIO
38	H2	BK7_IO_P18	T.B.D.	GPIO
39	J2	BK7_IO_N15	T.B.D.	GPIO
40	H1	BK7_IO_N18/VREF	T.B.D.	GPIO/Bank 7 VREF
41	J7	BK7_IO_P17	T.B.D.	GPIO
42	K2	BK7_IO_P12	T.B.D.	GPIO
43	C14	BK1_IO_P1/CLK4	T.B.D.	GPIO
44	K1	BK7_IO_N12	T.B.D.	GPIO/GCLK
45	B14	BK1_IO_N1/CLK5	T.B.D.	GPIO
46	L2	BK7_IO_P9	T.B.D.	GPIO/GCLK
47	K3	BK7_IO_N13	T.B.D.	GPIO
48	L1	BK7_IO_N9	T.B.D.	GPIO
49	K4	BK7_IO_P13	T.B.D.	GPIO
50	M2	BK7_IO_P5	T.B.D.	GPIO
51	K7	BK7_IO_N17	T.B.D.	GPIO
52	M1	BK7_IO_N5	T.B.D.	GPIO
53	L5	BK7_IO_N10	T.B.D.	GPIO
54	N2	BK7_IO_P1	T.B.D.	GPIO
55	L6	BK7_IO_P10	T.B.D.	GPIO
56	N1	BK7_IO_N1/VREF	T.B.D.	GPIO/Bank 7 VREF
57	--	GND	Ground	
58	--	GND		
59	--	VCC_7	Power supply for FPGA IO bank 7 can be taken from internal 2.5V, internal 3.3V, external JB4 or external JT1.	
60	--	VCC_7		
61	--	VCC_7		
62	--	VCC_7		
63	--	GND	Ground	
64	--	GND		
65	K6	BK7_IO_P14	T.B.D.	GPIO
66	N7	BK7_IO_N4	T.B.D.	GPIO
67	K5	BK7_IO_N14	T.B.D.	GPIO
68	N8	BK7_IO_P4	T.B.D.	GPIO
69	E4	BK7_IO_P29	T.B.D.	GPIO
70	L8	BK7_IO_P11/VREF	T.B.D.	GPIO/Bank 7 VREF
71	E3	BK7_IO_N29	T.B.D.	GPIO
72	L7	BK7_IO_N11	T.B.D.	GPIO
73	N3	BK7_IO_N2	T.B.D.	GPIO
74	--	NC	Not connected	
75	N4	BK7_IO_P2	T.B.D.	GPIO
76	--	NC	Not connected	
77	--	NC	Not connected	
78	--	NC	Not connected	
79	--	NC	Not connected	
80	--	NC	Not connected	
81	--	NC	Not connected	
82	--	NC	Not connected	
83	--	NC	Not connected	
84	--	NC	Not connected	

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
85	--	NC	Not connected	
86	--	NC	Not connected	
87	--	NC	Not connected	
88	--	NC	Not connected	
89	--	NC	Not connected	
90	--	NC	Not connected	
91	--	NC	Not connected	
92	--	NC	Not connected	
93	--	NC	Not connected	
94	--	NC	Not connected	
95	--	NC	Not connected	
96	--	NC	Not connected	
97	--	NC	Not connected	
98	--	NC	Not connected	
99	--	NC	Not connected	
100	--	NC	Not connected	
101	--	NC	Not connected	
102	--	NC	Not connected	
103	--	NC	Not connected	
104	--	NC	Not connected	
105	--	NC	Not connected	
106	--	NC	Not connected	
107	--	NC	Not connected	
108	--	NC	Not connected	
109	--	NC	Not connected	
110	--	NC	Not connected	
111	--	NC	Not connected	
112	--	NC	Not connected	
113	AF4	BK5_IO_S11	T.B.D.	GPIO
114	--	NC	Not connected	
115	AD12	BK5_IO_S3	T.B.D.	GPIO
116	--	NC	Not connected	
117	--	GND	Ground	
118	--	GND		
119	--	+3.3v	+3.3v power supply	
120	--	+3.3v		

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
121	--	+3.3v	+3.3v power supply	
122	--	+3.3v		
123	--	GND	Ground	
124	--	GND		
125	--	NC	Not Connected	
126	--	NC	Not Connected	
127	--	NC	Not Connected	
128	--	NC	Not Connected	
129	--	NC	Not Connected	
130	--	NC	Not Connected	
131	--	NC	Not Connected	
132	--	NC	Not Connected	
133	--	NC	Not Connected	
134	--	NC	Not Connected	
135	--	NC	Not Connected	
136	--	NC	Not Connected	
137	--	NC	Not Connected	
138	--	NC	Not Connected	
139	--	NC	Not Connected	
140	--	NC	Not Connected	
141	--	NC	Not Connected	
142	--	NC	Not Connected	
143	--	NC	Not Connected	
144	--	NC	Not Connected	
145	--	NC	Not Connected	
146	--	NC	Not Connected	
147	--	NC	Not Connected	
148	--	NC	Not Connected	

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
149	--	NC	Not Connected	
150	--	NC	Not Connected	
151	--	NC	Not Connected	
152	--	NC	Not Connected	
153	--	NC	Not Connected	
154	--	NC	Not Connected	
155	--	NC	Not Connected	
156	--	NC	Not Connected	
157	--	NC	Not Connected	
158	--	NC	Not Connected	
159	--	NC	Not Connected	
160	--	NC	Not Connected	
161	--	NC	Not Connected	
162	P23	BK3_IO_P2	T.B.D.	GPIO
163	--	NC	Not Connected	
164	P24	BK3_IO_N2	T.B.D.	GPIO
165	--	NC	Not Connected	
166	T21	BK3_IO_P10	T.B.D.	GPIO
167	R19	BK3_IO_P8	T.B.D.	GPIO
168	T22	BK3_IO_N10	T.B.D.	GPIO
169	R20	BK3_IO_N8	T.B.D.	GPIO
170	W24	BK3_IO_N19	T.B.D.	GPIO
171	T19	BK3_IO_P11	T.B.D.	GPIO
172	Y23	BK3_IO_N24*	T.B.D.	GPIO
173	T20	BK3_IO_N11	T.B.D.	GPIO
174	Y22	BK3_IO_P24*	T.B.D.	GPIO
175	P19	BK3_IO_P4	T.B.D.	GPIO
176	AA24	BK3_IO_N25*	T.B.D.	GPIO
177	--	GND	Ground	
178	--	GND		
179	--	VCC_3	Power supply for FPGA IO bank 3 can be taken from internal 2.5V, internal 3.3V, external JB2 or external JT2.	
180	--	VCC_3		
181	--	VCC_3		
182	--	VCC_3		
183	--	GND	Ground	
184	--	GND		
185	P20	BK3_IO_N4	T.B.D.	GPIO
186	P21	BK3_IO_P3	T.B.D.	GPIO
187	P25	BK3_IO_P1	T.B.D.	GPIO
188	P22	BK3_IO_N3	T.B.D.	GPIO
189	P26	BK3_IO_N1/VREF	T.B.D.	GPIO/Bank 3 VREF
190	R22	BK3_IO_N7	T.B.D.	GPIO
191	R25	BK3_IO_P5/VREF	T.B.D.	GPIO/Bank 3 VREF
192	R21	BK3_IO_P7	T.B.D.	GPIO
193	R26	BK3_IO_N5	T.B.D.	GPIO
194	R24	BK3_IO_N6	T.B.D.	GPIO
195	T25	BK3_IO_P9	T.B.D.	GPIO
196	T23	BK3_IO_P6	T.B.D.	GPIO
197	T26	BK3_IO_N9	T.B.D.	GPIO
198	U22	BK3_IO_N14	T.B.D.	GPIO
199	U25	BK3_IO_P12	T.B.D.	GPIO
200	U21	BK3_IO_P14/VREF	T.B.D.	GPIO/Bank 3 VREF
201	U26	BK3_IO_N12	T.B.D.	GPIO
202	U20	BK3_IO_N17	T.B.D.	GPIO
203	V25	BK3_IO_N15	T.B.D.	GPIO
204	V20	BK3_IO_P17	T.B.D.	GPIO
205	V24	BK3_IO_P15	T.B.D.	GPIO
206	V21	BK3_IO_N20	T.B.D.	GPIO
207	W26	BK3_IO_N18	T.B.D.	GPIO
208	W22	BK3_IO_P20	T.B.D.	GPIO
209	W25	BK3_IO_P18	T.B.D.	GPIO
210	W21	BK3_IO_N22*	T.B.D.	GPIO
211	Y26	BK3_IO_N21	T.B.D.	GPIO
212	W20	BK3_IO_P22*	T.B.D.	GPIO
213	Y25	BK3_IO_P21	T.B.D.	GPIO
214	Y21	BK3_IO_N27*	T.B.D.	GPIO
215	AA26	BK3_IO_N23*	T.B.D.	GPIO
216	Y20	BK3_IO_P27*	T.B.D.	GPIO
217	AA25	BK3_IO_P23/VREF*	T.B.D.	GPIO/Bank 3 VREF

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
218	AA22	BK3_IO_N30/VRP	T.B.D.	GPIO/Bank 3 VRP
219	AB26	BK3_IO_N26*	T.B.D.	GPIO
220	AA21	BK3_IO_P30/VRN	T.B.D.	GPIO/Bank 3 VRN
221	AB25	BK3_IO_P26*	T.B.D.	GPIO
222	AA23	BK3_IO_P25*	T.B.D.	GPIO
223	AC26	BK3_IO_N28	T.B.D.	GPIO
224	AB24	BK3_IO_N29/VREF	T.B.D.	GPIO/Bank 3 VREF
225	AC25	BK3_IO_P28	T.B.D.	GPIO
226	AB23	BK3_IO_P29	T.B.D.	GPIO
227	U24	BK3_IO_N13	T.B.D.	GPIO
228	--	GND	Ground	
229	U23	BK3_IO_P13		GPIO
230	--	TDI_U	JTAG input data of upper board	
231	V22	BK3_IO_P16		GPIO
232	--	TDO_U	JTAG output data of upper board	
233	V23	BK3_IO_N16	T.B.D.	GPIO
234	--	TMS	JTAG select signals	
235	W23	BK3_IO_P19/VREF	T.B.D.	GPIO/Bank 3 VREF
236	--	TCK	JTAG clock signal	
237	--	GND	Ground	
238	--	GND		
239	--	+3.3v	+3.3v power supply	
240	--	+3.3v		

4 IO modules

4.1 IOMODULE 1 (U14)

IO MODULE U14-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1A	AGND				
2A	+AVDD				
3A	AGND				
4A	-AVDD				
5A	GND				
6A	+3.3V				
7A	GND				
8A	+3.3V				
9A	GND				
10A	+3.3V				
11A	GND				
12A	GND				
13A	IO1_DA00				
14A	IO1_DA01				
15A	IO1_DA02				
16A	IO1_DA03				
17A	IO1_DA04				
18A	IO1_DA05				
19A	GND				
20A	GND				
21A	IO1_DA06				
22A	IO1_DA07				
23A	IO1_DA08				
24A	IO1_DA09				
25A	IO1_DA10				
26A	IO1_DA11				
27A	GND				
28A	GND				
29A	IO1_DA12				
30A	IO1_DA13				
31A	IO1_DA14				
32A	IO1_DA15				
33A	IO1_DA16				
34A	IO1_DA17				
35A	GND				
36A	GND				
37A	IO1_DA18				
38A	IO1_DA19				
39A	IO1_DA20				
40A	IO1_DA21				
41A	IO1_DA22				
42A	IO1_DA23				
43A	GND	--	--	--	--
44A	GND				
45A	IO1_DA24				
46A	IO1_DA25				
47A	IO1_DA26				
48A	IO1_DA27				
49A	IO1_DA28				
50A	IO1_DA29				
51A	GND				
52A	GND				
53A	IO1_DA30				
54A	IO1_DA31				
55A	IO1_DA32				
56A	IO1_DA33				
57A	IO1_DA34				
58A	IO1_DA35				
59A	GND				

IO MODULE U14-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
60A	GND				
61A	IO1_DA36				
62A	IO1_DA37				
63A	IO1_DA38				
64A	IO1_DA39				
65A	IO1_DA40				
66A	IO1_DA41				
67A	GND				
68A	GND				
69A	IO1_DA42				
70A	IO1_DA43				
71A	IO1_DA44				
72A	IO1_DA45				
73A	IO1_DA46				
74A	IO1_DA47				
75A	GND				
76A	GND				
77A	IO1_DA48				
78A	IO1_DA49				
79A	GND				
80A	GND				

IO MODULE U14-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1B	AGND				
2B	+AVDD				
3B	AGND				
4B	-AVDD				
5B	GND				
6B	+3.3V				
7B	GND				
8B	+3.3V				
9B	GND				
10B	+3.3V				
11B	GND				
12B	GND				
13B	IO1_DB00				
14B	IO1_DB01				
15B	IO1_DB02				
16B	IO1_DB03				
17B	IO1_DB04				
18B	IO1_DB05				
19B	GND				
20B	GND				
21B	IO1_DB06				
22B	IO1_DB07				
23B	IO1_DB08				
24B	IO1_DB09				
25B	IO1_DB10				
26B	IO1_DB11				
27B	GND				
28B	GND				
29B	IO1_DB12				
30B	IO1_DB13				
31B	IO1_DB14				
32B	IO1_DB15				
33B	IO1_DB16				
34B	IO1_DB17				
35B	GND				
36B	GND				
37B	IO1_DB18				
38B	IO1_DB19				
39B	IO1_DB20				
40B	IO1_DB21				
41B	IO1_DB22				

IO MODULE U14-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
42B	IO1_DB23				
43B	GND	--	--	--	--
44B	GND				
45B	IO1_DB24				
46B	IO1_DB25				
47B	IO1_DB26				
48B	IO1_DB27				
49B	IO1_DB28				
50B	IO1_DB29				
51B	GND				
52B	GND				
53B	IO1_DB30				
54B	IO1_DB31				
55B	IO1_DB32				
56B	IO1_DB33				
57B	IO1_DB34				
58B	IO1_DB35				
59B	GND				
60B	GND				
61B	IO1_DB36				
62B	IO1_DB37				
63B	IO1_DB38				
64B	IO1_DB39				
65B	IO1_DB40				
66B	IO1_DB41				
67B	GND				
68B	GND				
69B	IO1_DB42				
70B	IO1_DB43				
71B	IO1_DB44				
72B	IO1_DB45				
73B	IO1_DB46				
74B	IO1_DB47				
75B	GND				
76B	GND				
77B	IO1_DB48				
78B	IO1_DB49				
79B	GND				
80B	GND				

4.2 IOMODULE 2 (U38)

IO MODULE U38-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1A	AGND				
2A	+AVDD				
3A	AGND				
4A	-AVDD				
5A	GND				
6A	+3.3V				
7A	GND				
8A	+3.3V				
9A	GND				
10A	+3.3V				
11A	GND				
12A	GND				
13A	IO2_DA00				
14A	IO2_DA01				
15A	IO2_DA02				
16A	IO2_DA03				
17A	IO2_DA04				
18A	IO2_DA05				
19A	GND				

IO MODULE U38-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
20A	GND				
21A	IO2_DA06				
22A	IO2_DA07				
23A	IO2_DA08				
24A	IO2_DA09				
25A	IO2_DA10				
26A	IO2_DA11				
27A	GND				
28A	GND				
29A	IO2_DA12				
30A	IO2_DA13				
31A	IO2_DA14				
32A	IO2_DA15				
33A	IO2_DA16				
34A	IO2_DA17				
35A	GND				
36A	GND				
37A	IO2_DA18				
38A	IO2_DA19				
39A	IO2_DA20				
40A	IO2_DA21				
41A	IO2_DA22				
42A	IO2_DA23				
43A	GND	--	--	--	--
44A	GND				
45A	IO2_DA24				
46A	IO2_DA25				
47A	IO2_DA26				
48A	IO2_DA27				
49A	IO2_DA28				
50A	IO2_DA29				
51A	GND				
52A	GND				
53A	IO2_DA30				
54A	IO2_DA31				
55A	IO2_DA32				
56A	IO2_DA33				
57A	IO2_DA34				
58A	IO2_DA35				
59A	GND				
60A	GND				
61A	IO2_DA36				
62A	IO2_DA37				
63A	IO2_DA38				
64A	IO2_DA39				
65A	IO2_DA40				
66A	IO2_DA41				
67A	GND				
68A	GND				
69A	IO2_DA42				
70A	IO2_DA43				
71A	IO2_DA44				
72A	IO2_DA45				
73A	IO2_DA46				
74A	IO2_DA47				
75A	GND				
76A	GND				
77A	IO2_DA48				
78A	IO2_DA49				
79A	GND				
80A	GND				

IO MODULE U38-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1B	AGND				

IO MODULE U38-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
2B	+AVDD				
3B	AGND				
4B	-AVDD				
5B	GND				
6B	+3.3V				
7B	GND				
8B	+3.3V				
9B	GND				
10B	+3.3V				
11B	GND				
12B	GND				
13B	IO2_DB00				
14B	IO2_DB01				
15B	IO2_DB02				
16B	IO2_DB03				
17B	IO2_DB04				
18B	IO2_DB05				
19B	GND				
20B	GND				
21B	IO2_DB06				
22B	IO2_DB07				
23B	IO2_DB08				
24B	IO2_DB09				
25B	IO2_DB10				
26B	IO2_DB11				
27B	GND				
28B	GND				
29B	IO2_DB12				
30B	IO2_DB13				
31B	IO2_DB14				
32B	IO2_DB15				
33B	IO2_DB16				
34B	IO2_DB17				
35B	GND				
36B	GND				
37B	IO2_DB18				
38B	IO2_DB19				
39B	IO2_DB20				
40B	IO2_DB21				
41B	IO2_DB22				
42B	IO2_DB23				
43B	GND	--	--	--	--
44B	GND				
45B	IO2_DB24				
46B	IO2_DB25				
47B	IO2_DB26				
48B	IO2_DB27				
49B	IO2_DB28				
50B	IO2_DB29				
51B	GND				
52B	GND				
53B	IO2_DB30				
54B	IO2_DB31				
55B	IO2_DB32				
56B	IO2_DB33				
57B	IO2_DB34				
58B	IO2_DB35				
59B	GND				
60B	GND				
61B	IO2_DB36				
62B	IO2_DB37				
63B	IO2_DB38				
64B	IO2_DB39				
65B	IO2_DB40				
66B	IO2_DB41				
67B	GND				
68B	GND				
69B	IO2_DB42				
70B	IO2_DB43				
71B	IO2_DB44				

IO MODULE U38-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
72B	IO2_DB45				
73B	IO2_DB46				
74B	IO2_DB47				
75B	GND				
76B	GND				
77B	IO2_DB48				
78B	IO2_DB49				
79B	GND				
80B	GND				

4.3 IOMODULE 3 (U24)

IO module 3 shares connector A with connector B of IO Module 2.

IO MODULE U24-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1A	AGND				
2A	+AVDD				
3A	AGND				
4A	-AVDD				
5A	GND				
6A	+3.3V				
7A	GND				
8A	+3.3V				
9A	GND				
10A	+3.3V				
11A	GND				
12A	GND				
13A	IO2_DB00				
14A	IO2_DB01				
15A	IO2_DB02				
16A	IO2_DB03				
17A	IO2_DB04				
18A	IO2_DB05				
19A	GND				
20A	GND				
21A	IO2_DB06				
22A	IO2_DB07				
23A	IO2_DB08				
24A	IO2_DB09				
25A	IO2_DB10				
26A	IO2_DB11				
27A	GND				
28A	GND				
29A	IO2_DB12				
30A	IO2_DB13				
31A	IO2_DB14				
32A	IO2_DB15				
33A	IO2_DB16				
34A	IO2_DB17				
35A	GND				
36A	GND				
37A	IO2_DB18				
38A	IO2_DB19				
39A	IO2_DB20				
40A	IO2_DB21				
41A	IO2_DB22				
42A	IO2_DB23				
43A	GND	--	--	--	--
44A	GND				
45A	IO2_DB24				
46A	IO2_DB25				
47A	IO2_DB26				

IO MODULE U24-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
48A	IO2_DB27				
49A	IO2_DB28				
50A	IO2_DB29				
51A	GND				
52A	GND				
53A	IO2_DB30				
54A	IO2_DB31				
55A	IO2_DB32				
56A	IO2_DB33				
57A	IO2_DB34				
58A	IO2_DB35				
59A	GND				
60A	GND				
61A	IO2_DB36				
62A	IO2_DB37				
63A	IO2_DB38				
64A	IO2_DB39				
65A	IO2_DB40				
66A	IO2_DB41				
67A	GND				
68A	GND				
69A	IO2_DB42				
70A	IO2_DB43				
71A	IO2_DB44				
72A	IO2_DB45				
73A	IO2_DB46				
74A	IO2_DB47				
75A	GND				
76A	GND				
77A	IO2_DB48				
78A	IO2_DB49				
79A	GND				
80A	GND				

IO MODULE U24-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1B	AGND				
2B	+AVDD				
3B	AGND				
4B	-AVDD				
5B	GND				
6B	+3.3V				
7B	GND				
8B	+3.3V				
9B	GND				
10B	+3.3V				
11B	GND				
12B	GND				
13B	IO3_DB00				
14B	IO3_DB01				
15B	IO3_DB02				
16B	IO3_DB03				
17B	IO3_DB04				
18B	IO3_DB05				
19B	GND				
20B	GND				
21B	IO3_DB06				
22B	IO3_DB07				
23B	IO3_DB08				
24B	IO3_DB09				
25B	IO3_DB10				
26B	IO3_DB11				
27B	GND				
28B	GND				
29B	IO3_DB12				

IO MODULE U24-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
30B	IO3_DB13				
31B	IO3_DB14				
32B	IO3_DB15				
33B	IO3_DB16				
34B	IO3_DB17				
35B	GND				
36B	GND				
37B	IO3_DB18				
38B	IO3_DB19				
39B	IO3_DB20				
40B	IO3_DB21				
41B	IO3_DB22				
42B	IO3_DB23				
43B	GND	--	--	--	--
44B	GND				
45B	IO3_DB24				
46B	IO3_DB25				
47B	IO3_DB26				
48B	IO3_DB27				
49B	IO3_DB28				
50B	IO3_DB29				
51B	GND				
52B	GND				
53B	IO3_DB30				
54B	IO3_DB31				
55B	IO3_DB32				
56B	IO3_DB33				
57B	IO3_DB34				
58B	IO3_DB35				
59B	GND				
60B	GND				
61B	IO3_DB36				
62B	IO3_DB37				
63B	IO3_DB38				
64B	IO3_DB39				
65B	IO3_DB40				
66B	IO3_DB41				
67B	GND				
68B	GND				
69B	IO3_DB42				
70B	IO3_DB43				
71B	IO3_DB44				
72B	IO3_DB45				
73B	IO3_DB46				
74B	IO3_DB47				
75B	GND				
76B	GND				
77B	IO3_DB48				
78B	IO3_DB49				
79B	GND				
80B	GND				

4.4 IOMODULE 4 (U25)

IO module 4 shares connector A with connector B of IO Module 1.

IO MODULE U24-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1A	AGND				
2A	+AVDD				
3A	AGND				
4A	-AVDD				
5A	GND				
6A	+3.3V				
7A	GND				

IO MODULE U24-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
8A	+3.3V				
9A	GND				
10A	+3.3V				
11A	GND				
12A	GND				
13A	IO1_DB00				
14A	IO1_DB01				
15A	IO1_DB02				
16A	IO1_DB03				
17A	IO1_DB04				
18A	IO1_DB05				
19A	GND				
20A	GND				
21A	IO1_DB06				
22A	IO1_DB07				
23A	IO1_DB08				
24A	IO1_DB09				
25A	IO1_DB10				
26A	IO1_DB11				
27A	GND				
28A	GND				
29A	IO1_DB12				
30A	IO1_DB13				
31A	IO1_DB14				
32A	IO1_DB15				
33A	IO1_DB16				
34A	IO1_DB17				
35A	GND				
36A	GND				
37A	IO1_DB18				
38A	IO1_DB19				
39A	IO1_DB20				
40A	IO1_DB21				
41A	IO1_DB22				
42A	IO1_DB23				
43A	GND	--	--	--	--
44A	GND				
45A	IO1_DB24				
46A	IO1_DB25				
47A	IO1_DB26				
48A	IO1_DB27				
49A	IO1_DB28				
50A	IO1_DB29				
51A	GND				
52A	GND				
53A	IO1_DB30				
54A	IO1_DB31				
55A	IO1_DB32				
56A	IO1_DB33				
57A	IO1_DB34				
58A	IO1_DB35				
59A	GND				
60A	GND				
61A	IO1_DB36				
62A	IO1_DB37				
63A	IO1_DB38				
64A	IO1_DB39				
65A	IO1_DB40				
66A	IO1_DB41				
67A	GND				
68A	GND				
69A	IO1_DB42				
70A	IO1_DB43				
71A	IO1_DB44				
72A	IO1_DB45				
73A	IO1_DB46				
74A	IO1_DB47				
75A	GND				
76A	GND				
77A	IO2_DB48				

IO MODULE U24-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
78A	IO1_DB49				
79A	GND				
80A	GND				

IO MODULE U24-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1B	AGND				
2B	+AVDD				
3B	AGND				
4B	-AVDD				
5B	GND				
6B	+3.3V				
7B	GND				
8B	+3.3V				
9B	GND				
10B	+3.3V				
11B	GND				
12B	GND				
13B	IO4_DB00				
14B	IO4_DB01				
15B	IO4_DB02				
16B	IO4_DB03				
17B	IO4_DB04				
18B	IO4_DB05				
19B	GND				
20B	GND				
21B	IO4_DB06				
22B	IO4_DB07				
23B	IO4_DB08				
24B	IO4_DB09				
25B	IO4_DB10				
26B	IO4_DB11				
27B	GND				
28B	GND				
29B	IO4_DB12				
30B	IO4_DB13				
31B	IO4_DB14				
32B	IO4_DB15				
33B	IO4_DB16				
34B	IO4_DB17				
35B	GND				
36B	GND				
37B	IO4_DB18				
38B	IO4_DB19				
39B	IO4_DB20				
40B	IO4_DB21				
41B	IO4_DB22				
42B	IO4_DB23				
43B	GND	--	--	--	--
44B	GND				
45B	IO4_DB24				
46B	IO4_DB25				
47B	IO4_DB26				
48B	IO3_DB27				
49B	IO4_DB28				
50B	IO4_DB29				
51B	GND				
52B	GND				
53B	IO4_DB30				
54B	IO4_DB31				
55B	IO4_DB32				
56B	IO4_DB33				
57B	IO4_DB34				
58B	IO4_DB35				
59B	GND				

IO MODULE U24-B		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
60B	GND				
61B	IO4_DB36				
62B	IO4_DB37				
63B	IO4_DB38				
64B	IO4_DB39				
65B	IO4_DB40				
66B	IO4_DB41				
67B	GND				
68B	GND				
69B	IO4_DB42				
70B	IO4_DB43				
71B	IO4_DB44				
72B	IO4_DB45				
73B	IO4_DB46				
74B	IO4_DB47				
75B	GND				
76B	GND				
77B	IO4_DB48				
78B	IO4_DB49				
79B	GND				
80B	GND				

5 VIDEO IO

5.1 Analog Video input

PROTONV2-3M07 contains the ANALOG DEVICES video decoder ADV7180 (position U20) as one of the analog video inputs of the system. The ADV7180 automatically detects and converts standard analog baseband television signals compatible with NTSC, PAL, and SECAM standards into 4:2:2 component video data compatible with the 8-bit ITU-R BT.656 interface standard. 10-bit accurate A/D conversion provides professional quality video performance with true 8-bit data resolution. Three analog video input channels accept standard Composite, S-Video, or YPrPb video signals, supporting a wide range of consumer video sources. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 1 V. Alternatively, these can be bypassed for manual settings.

Figure below shows the FPGA lines assigned to the analog video input of the system. The digital lines assignment is complete.

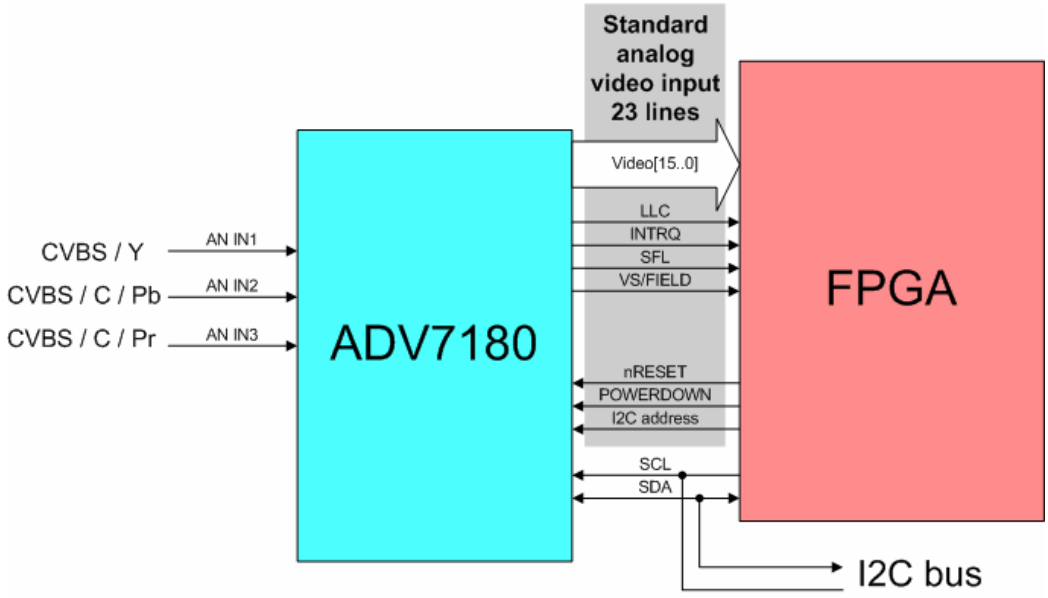

Figure 7. *FPGA lines used for the standard analog video interface (position U20).*

5.2 Analog Video Output

PROTONV2-3M07 outputs three different high speed analog signals controlled by the FPGA module of the system using a Texas Instruments THS8133 digital to analog converter. These

three signals can drive a standard PC monitor, be used for generating analog video format or as generic signal generator.

The THS8133 is a general-purpose triple high-speed digital to analog converter optimized for use in video/graphics applications. The device operates from a 5-V analog supply and a 3-V to 5-V range digital supply. The THS8133 has a sampling rate up to 80 MSPS. The device consists of three 10-bit D/A converters and additional circuitry for bi-level/tri-level sync and blanking level generation in video applications.

THS8133 is also well suited in applications where multiple well-matched and synchronously operating DACs are needed; for example, I-Q modulation and direct-digital synthesis in communications equipment. The current-steering DACs can be directly terminated in resistive loads to produce voltage outputs. The device provides a flexible configuration of maximum output current drive. Its output drivers are specifically designed to produce standard video output levels when directly connected to a single-ended doubly-terminated 75 Ω coaxial cable. Full-scale video/sync are generated in a 7:3 ratio, compliant with SMPTE standards for YPbPr signals. Furthermore, the THS8133 can generate both; a traditional bi-level sync or a tri-level sync signal, as per the SMPTE standards, via a digital control interface. The sync signal is inserted on one of the analog output channels (sync-on-green/luminance) or on all output channels. Also, a blanking control signal sets the outputs to defined levels during the nonactive video window.

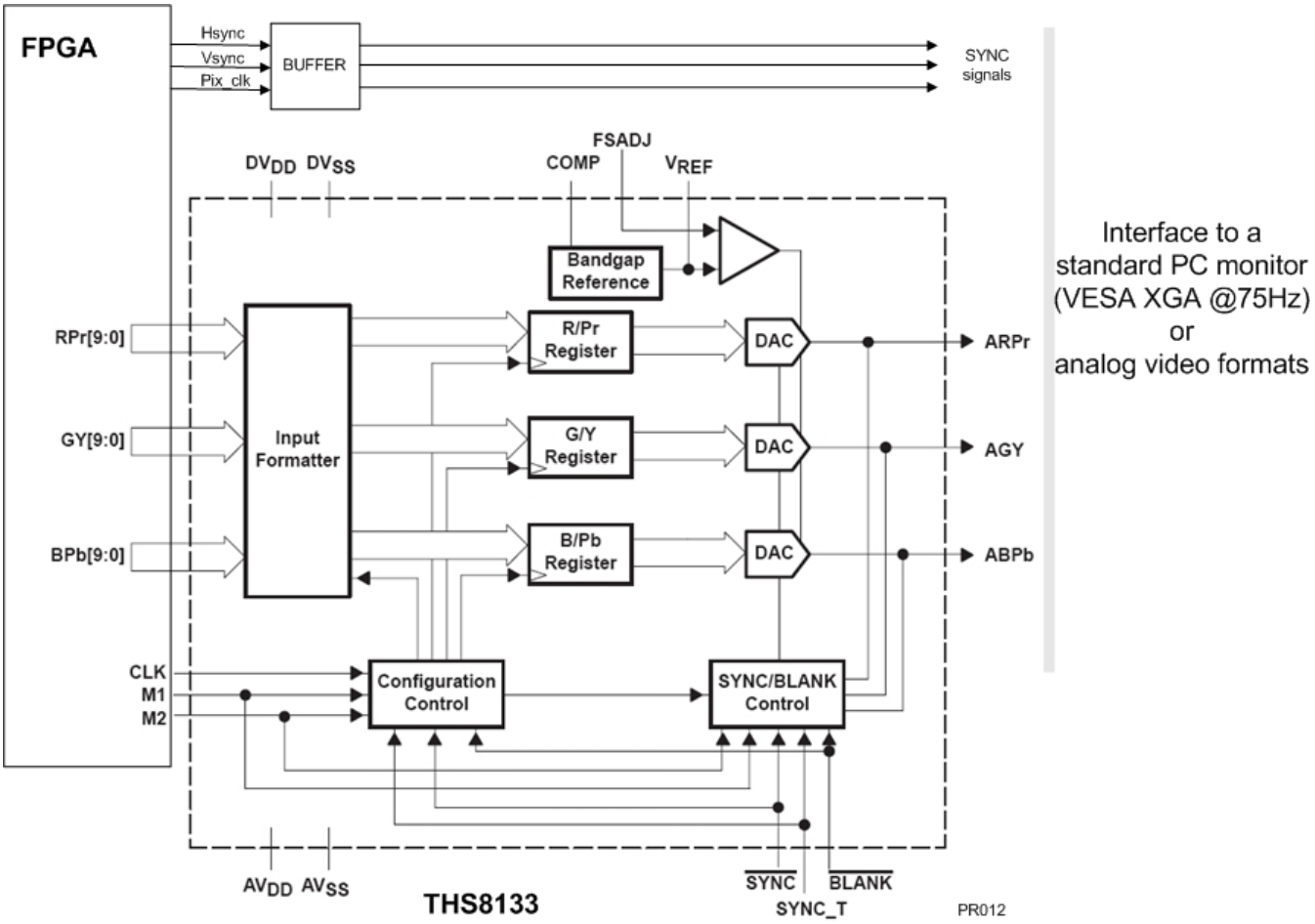

Figure 8. *Analog video output.*

5.3 DVI and RGB input

PROTONV2-3M07 captures video data output from a PC graphics card using Single Link DVI-I interface where digital TMDS and Analog RGB are available with a resolution of up to 1600x1200@60Hz and a color depth of 24 bits.

An Analog Devices AD9887A is used for grabbing data from DVI-I (Single Link) interface.

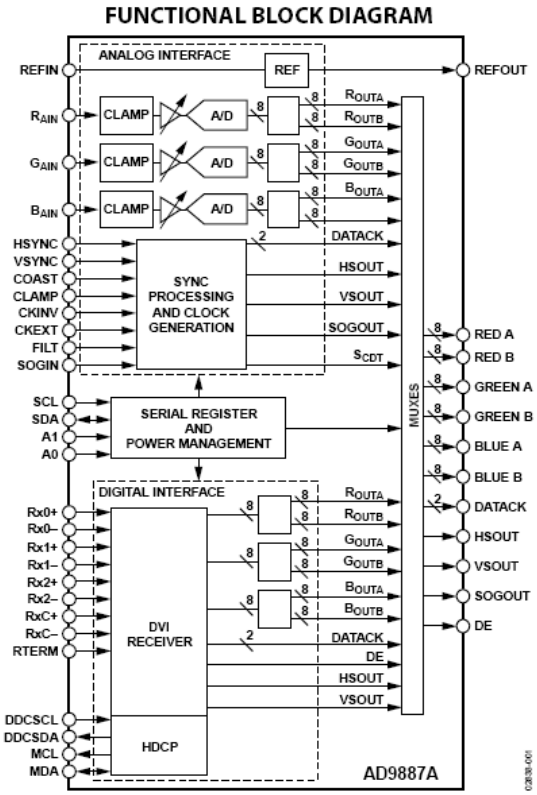

Figure 9. *AD9887A dual interface for Flat panel display.*

5.4 DVI out

TBD

6 JTAG chain

The position J4 is a JTAG connector. Cables like the XILINX parallel III can be used to program the devices present in the PROTONV2-3M07 hardware.

The user can program:

- Configuration PROM in FPGA modules.
- FPGA's of the system.
- Flash memory device in the microcontroller module.

The following figure indicates the order of the JTAG connector pins and its relative position to other components on the PCB.

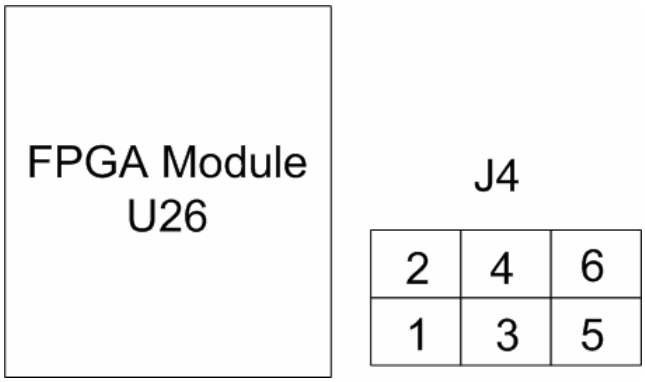

Figure 10. *Pin location of the JTAG connector on PROTONV2-3M07*

J4 pin	Signal name	U37 pin	Signal name
1	TDO	2	TDI
4	TCK	4	TMS
5	+3.3v	6	GND

Resistor jumpers R65, R66, R67, R68 and R69 configure the JTAG chain in PROTONV2-3M07 system. Next table summarises the JTAG chain options.

OPTION	RESISTOR/JUMPER	
ONLY FPGA in the chain	R69 - 0R	NO
	R65 - 0R	YES
	R66 - 0R	NO
	R67 - 0R	YES
	R68 - 0R	NO
ONLY microcontroller module in the chain	R69 - 0R	NO
	R65 - 0R	NO
	R66 - 0R	YES
	R67 - 0R	NO
	R68 - 0R	YES
microcontroller and PFGA module in the chain	R69 - 0R	YES
	R65 - 0R	YES
	R66 - 0R	NO
	R67 - 0R	NO
	R68 - 0R	YES

7 Physical dimensions and footprints

7.1 IO MODULE.

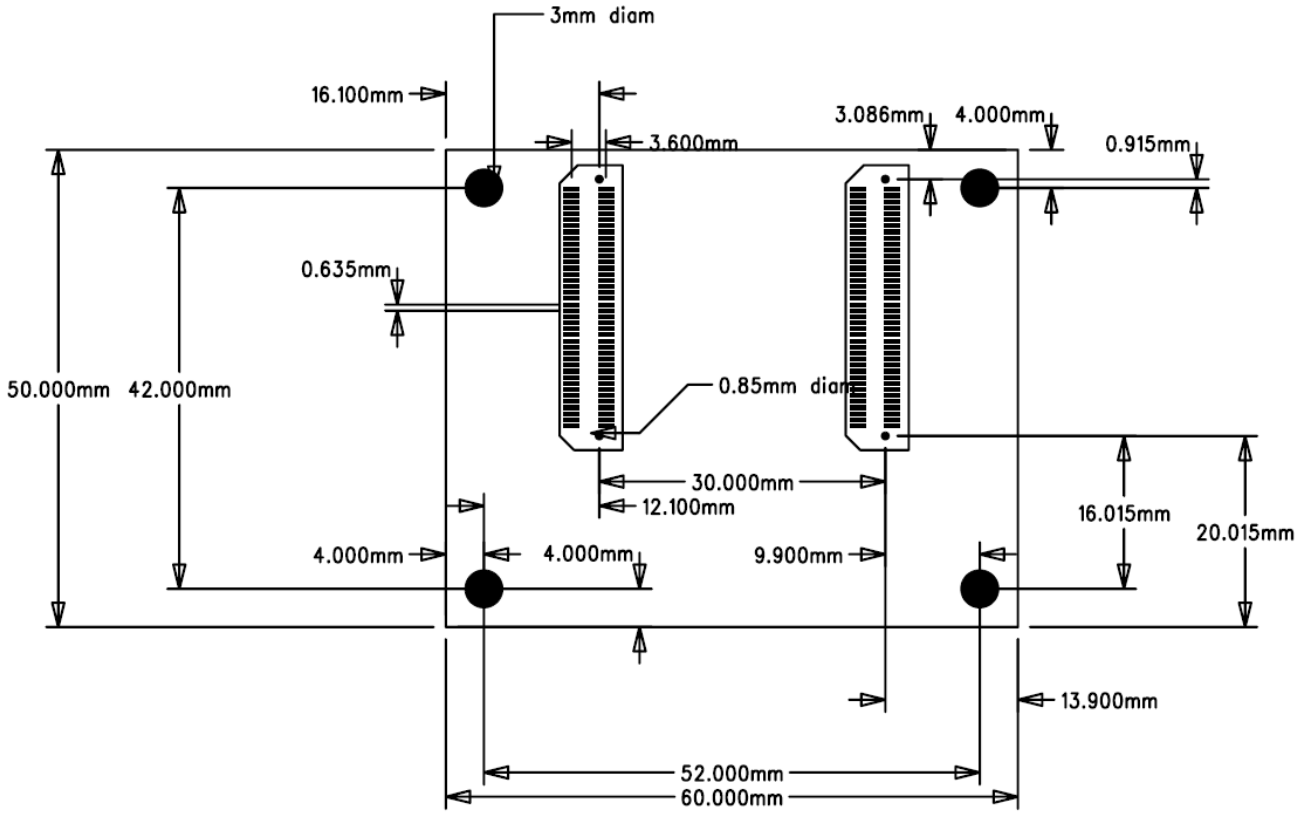

Figure 11.*IO Module dimension.*

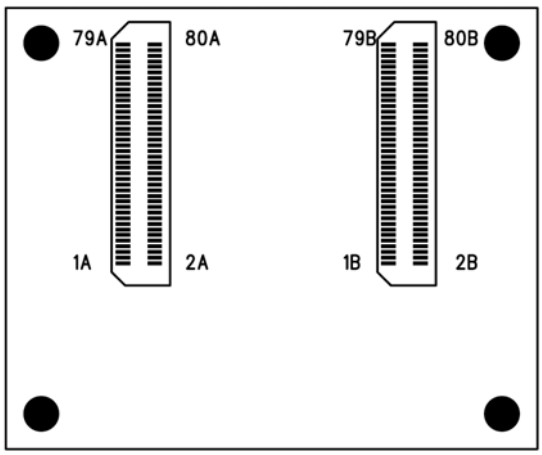

Figure 12. *IO Module pin position.*

7.2 FPGA MODULE

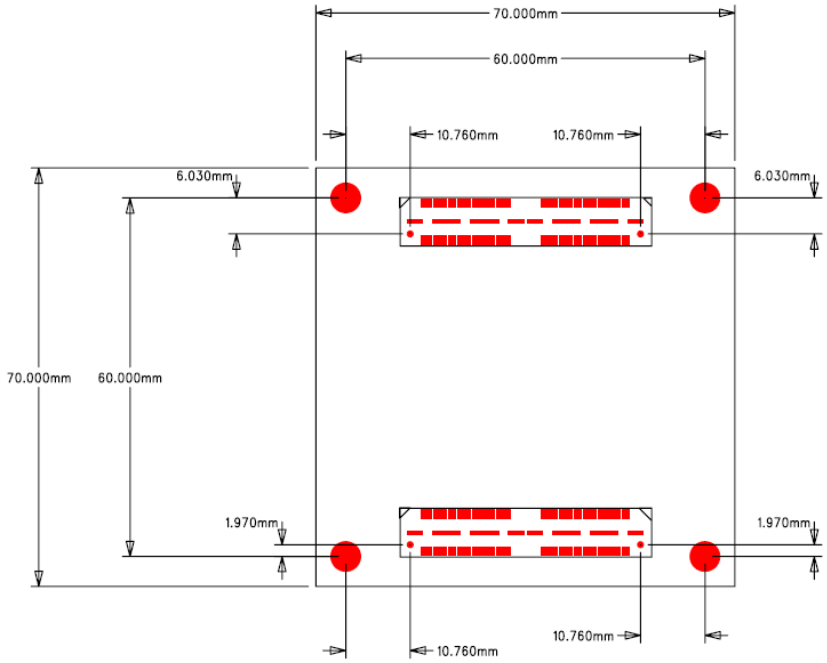

Figure 13. *FPGA Module Top layer dimensions.*

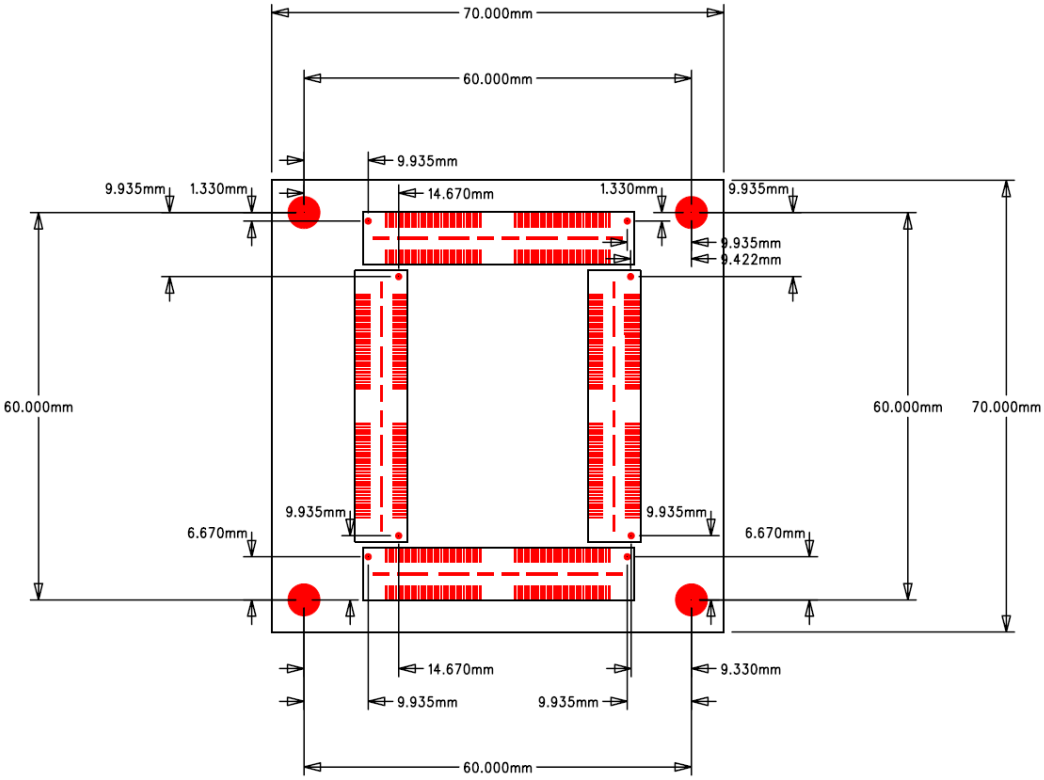

Figure 14. *FPGA Module Bottom layer dimensions.*

8 Accessories

The following devices are available for complementing PROTONV2-3M07.

8.1 SDRAM MODULE

SDRAM module can be plugged on top of the FPGA module contains the following resources:

Qty.	Position	Resource	Description
1	U15	SODIMM 144	144 pin socket suitable for plugging a standard SDRAM SODIMM-144
1	U2	Flat cable connector	Flat cable connector for driving a Hitachi LCD module TX09D70VM1CCA.
1	U3	Touch screen controller	Philips UCB1400 touch screen controller and audio coder.
2	U1-A, U1-B	120 pin SAMTEC connector	Connectors compatible to FPGA module.

The connectors (U1-A and U1-B) on the bottom layer, supply 3.3v to the module and connect the SDRAM SODIMM lines, LCD signals and Touch controller signals to the FPGA of the system. Next tables list the pin assignment of these connectors.

SDRAM module U1-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1	+3.3v	--	+3.3v	+3.3v power supply	
2	+3.3v	--	+3.3v		
3	GND	--	GND	Ground	
4	GND	--	GND		
5	SD_DQ20	F5	BK7_IO_N30/VRP	SDRAM data bus, bit 20	GPIO
6	SD_DQ19	H5	BK7_IO_P20/VREF	SDRAM data bus, bit 19	GPIO
7	SD_DQ21	F6	BK7_IO_P30/VRN	SDRAM data bus, bit 21	GPIO
8	SD_DQ18	J6	BK7_IO_N20	SDRAM data bus, bit 18	GPIO
9	SD_DQ22	G6	BK7_IO_N27*	SDRAM data bus, bit 22	GPIO
10	SD_DQ17	J5	BK7_IO_P16	SDRAM data bus, bit 17	GPIO
11	SD_DQ23	G7	BK7_IO_P27*	SDRAM data bus, bit 23	GPIO
12	SD_DQ16	J4	BK7_IO_N16	SDRAM data bus, bit 16	GPIO
13	SD_DQ24	H6	BK7_IO_N22*	SDRAM data bus, bit 24	GPIO
14	SD_DQ15	M7	BK7_IO_N8	SDRAM data bus, bit 15	GPIO
15	SD_DQ25	H7	BK7_IO_P22/VREF*	SDRAM data bus, bit 25	GPIO
16	SD_DQ14	M8	BK7_IO_P8	SDRAM data bus, bit 14	GPIO
17	SD_DQ26	N5	BK7_IO_N3	SDRAM data bus, bit 26	GPIO
18	SD_DQ13	M6	BK7_IO_N7	SDRAM data bus, bit 13	GPIO
19	SD_DQ27	N6	BK7_IO_P3	SDRAM data bus, bit 27	GPIO
20	SD_DQ47	M5	BK7_IO_P7	SDRAM data bus, bit 47	GPIO
21	SD_DQ31	F4	BK7_IO_P25*	SDRAM data bus, bit 31	GPIO
22	SD_DQ46	D2	BK7_IO_P28	SDRAM data bus, bit 46	GPIO
23	SD_DQ30	F3	BK7_IO_N25*	SDRAM data bus, bit 30	GPIO
24	SD_DQ45	D1	BK7_IO_N28/VREF	SDRAM data bus, bit 45	GPIO
25	SD_DQ29	G5	BK7_IO_P24*	SDRAM data bus, bit 29	GPIO
26	SD_DQ44	E2	BK7_IO_P26*	SDRAM data bus, bit 44	GPIO
27	SD_DQ28	G4	BK7_IO_N24*	SDRAM data bus, bit 28	GPIO
28	SD_DQ12	E1	BK7_IO_N26*	SDRAM data bus, bit 12	GPIO
29	SD_DQ59	L4	BK7_IO_P6	SDRAM data bus, bit 59	GPIO
30	SD_DQ11	F2	BK7_IO_P23*	SDRAM data bus, bit 11	GPIO
31	SD_DQ58	M3	BK7_IO_N6	SDRAM data bus, bit 58	GPIO
32	SD_DQ43	F1	BK7_IO_N23*	SDRAM data bus, bit 43	GPIO
33	SD_DQ57	H3	BK7_IO_N19	SDRAM data bus, bit 57	GPIO
34	SD_DQ42	G2	BK7_IO_P21	SDRAM data bus, bit 42	GPIO
35	SD_DQ56	H4	BK7_IO_P19	SDRAM data bus, bit 56	GPIO

SDRAM module U1-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
36	SD_DQ10	G1	BK7_IO_N21	SDRAM data bus, bit 10	GPIO
37	SD_DQ55	J3	BK7_IO_P15	SDRAM data bus, bit 55	GPIO
38	SD_DQ09	H2	BK7_IO_P18	SDRAM data bus, bit 09	GPIO
39	SD_DQ54	J2	BK7_IO_N15	SDRAM data bus, bit 54	GPIO
40	SD_DQ08	H1	BK7_IO_N18/VREF	SDRAM data bus, bit 08	GPIO
41	SD_DQ53	J7	BK7_IO_P17	SDRAM data bus, bit 53	GPIO
42	SD_DQ07	K2	BK7_IO_P12	SDRAM data bus, bit 07	GPIO
43	SD_CLK0_R	C14	BK1_IO_P1/CLK4	SDRAM clock signal 0	GPIO
44	SD_DQ06	K1	BK7_IO_N12	SDRAM data bus, bit 6	GPIO/GCLK
45	SD_CLK1_R	B14	BK1_IO_N1/CLK5	SDRAM clock signal 1	GPIO
46	SD_DQ05	L2	BK7_IO_P9	SDRAM data bus, bit 5	GPIO/GCLK
47	SD_DQ52	K3	BK7_IO_N13	SDRAM data bus, bit 52	GPIO
48	SD_DQ04	L1	BK7_IO_N9	SDRAM data bus, bit 4	GPIO
49	SD_DQ51	K4	BK7_IO_P13	SDRAM data bus, bit 51	GPIO
50	SD_DQ03	M2	BK7_IO_P5	SDRAM data bus, bit 03	GPIO
51	SD_DQ50	K7	BK7_IO_N17	SDRAM data bus, bit 50	GPIO
52	SD_DQ02	M1	BK7_IO_N5	SDRAM data bus, bit 02	GPIO
53	SD_DQ49	L5	BK7_IO_N10	SDRAM data bus, bit 49	GPIO
54	SD_DQ01	N2	BK7_IO_P1	SDRAM data bus, bit 1	GPIO
55	SD_DQ48	L6	BK7_IO_P10	SDRAM data bus, bit 48	GPIO
56	SD_DQ00	N1	BK7_IO_N1/VREF	SDRAM data bus, bit 0	GPIO
57	GND	--	GND	Ground	
58	GND	--	GND		
59	+3.3v	--	VCC_7	Power supply for FPGA IO bank 7	
60	+3.3v	--	VCC_7		
61	+3.3v	--	VCC_7		
62	+3.3v	--	VCC_7		
63	GND	--	GND	Ground	
64	GND	--	GND		
65	SD_DQ37	K6	BK7_IO_P14	SDRAM data bus, bit 37	GPIO
66	SD_DQ41	N7	BK7_IO_N4	SDRAM data bus, bit 41	GPIO
67	SD_DQ36	K5	BK7_IO_N14	SDRAM data bus, bit 36	GPIO
68	SD_DQ40	N8	BK7_IO_P4	SDRAM data bus, bit 40	GPIO
69	SD_DQ35	E4	BK7_IO_P29	SDRAM data bus, bit 35	GPIO
70	SD_DQ39	L8	BK7_IO_P11/VREF	SDRAM data bus, bit 39	GPIO
71	SD_DQ32	E3	BK7_IO_N29	SDRAM data bus, bit 32	GPIO
72	SD_DQ38	L7	BK7_IO_N11	SDRAM data bus, bit 38	GPIO
73	SD_DQ33	N3	BK7_IO_N2	SDRAM data bus, bit 33	GPIO
74	NC	--	NC	Not connected	
75	SD_DQ34	N4	BK7_IO_P2	SDRAM data bus, bit 34	GPIO
76	NC	--	NC	Not connected	
77	NC	--	NC	Not connected	
78	NC	--	NC	Not connected	
79	NC	--	NC	Not connected	
80	NC	--	NC	Not connected	
81	NC	--	NC	Not connected	
82	NC	--	NC	Not connected	
83	NC	--	NC	Not connected	
84	NC	--	NC	Not connected	
85	NC	--	NC	Not connected	
86	NC	--	NC	Not connected	
87	NC	--	NC	Not connected	
88	NC	--	NC	Not connected	
89	NC	--	NC	Not connected	
90	NC	--	NC	Not connected	
91	NC	--	NC	Not connected	
92	NC	--	NC	Not connected	
93	NC	--	NC	Not connected	
94	NC	--	NC	Not connected	
95	NC	--	NC	Not connected	
96	NC	--	NC	Not connected	
97	NC	--	NC	Not connected	
98	NC	--	NC	Not connected	
99	NC	--	NC	Not connected	
100	NC	--	NC	Not connected	
101	NC	--	NC	Not connected	
102	NC	--	NC	Not connected	
103	NC	--	NC	Not connected	
104	NC	--	NC	Not connected	
105	NC	--	NC	Not connected	

SDRAM module U1-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
106	NC	--	NC	Not connected	
107	NC	--	NC	Not connected	
108	NC	--	NC	Not connected	
109	NC	--	NC	Not connected	
110	NC	--	NC	Not connected	
111	NC	--	NC	Not connected	
112	NC	--	NC	Not connected	
113	SCL/UCB_ADCSYNC	AF4	BK5_IO_S11	Selectable via 0 ohm resistor R23/R26 • I2C bus clock signal • UCB touch screen controller ADCSYNC	GPIO
114	NC	--	NC	Not connected	
115	SDA/UCB_IRQOUT	AD12	BK5_IO_S3	Selectable via 0 ohm resistor R27/R28 • I2C bus data signal • UCB touch screen controller interrupt signal	GPIO
116	NC	--	NC	Not connected	
117	GND	--	GND	Ground	
118	GND	--	GND		
119	+3.3v	--	+3.3v	+3.3v power supply	
120	+3.3v	--	+3.3v		

SDRAM module U1-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
121	+3.3v	--	+3.3v	+3.3v power supply	
122	+3.3v	--	+3.3v		
123	GND	--	GND	Ground	
124	GND	--	GND		
125	NC	--	NC	Not Connected	
126	NC	--	NC	Not Connected	
127	NC	--	NC	Not Connected	
128	NC	--	NC	Not Connected	
129	NC	--	NC	Not Connected	
130	NC	--	NC	Not Connected	
131	NC	--	NC	Not Connected	
132	NC	--	NC	Not Connected	
133	NC	--	NC	Not Connected	
134	NC	--	NC	Not Connected	
135	NC	--	NC	Not Connected	
136	NC	--	NC	Not Connected	
137	NC	--	NC	Not Connected	
138	NC	--	NC	Not Connected	
139	NC	--	NC	Not Connected	
140	NC	--	NC	Not Connected	
141	NC	--	NC	Not Connected	
142	NC	--	NC	Not Connected	
143	NC	--	NC	Not Connected	
144	NC	--	NC	Not Connected	
145	NC	--	NC	Not Connected	
146	NC	--	NC	Not Connected	
147	NC	--	NC	Not Connected	
148	NC	--	NC	Not Connected	
149	NC	--	NC	Not Connected	
150	NC	--	NC	Not Connected	
151	NC	--	NC	Not Connected	
152	NC	--	NC	Not Connected	
153	NC	--	NC	Not Connected	
154	NC	--	NC	Not Connected	
155	NC	--	NC	Not Connected	
156	NC	--	NC	Not Connected	
157	NC	--	NC	Not Connected	
158	NC	--	NC	Not Connected	
159	NC	--	NC	Not Connected	
160	NC	--	NC	Not Connected	
161	NC	--	NC	Not Connected	
162	SD_BA0	P23	BK3_IO_P2	SDRAM bank select 0	GPIO
163	NC	--	NC	Not Connected	

SDRAM module U1-A		FPGA		Description		
Pin	NAME	Pin	Name	System	FPGA module	
164	SD_BA1	P24	BK3_IO_N2	SDRAM bank select 1		GPIO
165	NC	--	NC	Not Connected		
166	SD_DQMB6	T21	BK3_IO_P10	SDRAM data mask byte 6		GPIO
167	SD_ADD_R11	R19	BK3_IO_P8	SDRAM address bus, bit 11		GPIO
168	SD_DQMB7	T22	BK3_IO_N10	SDRAM data mask byte 7		GPIO
169	SD_ADD_R10	R20	BK3_IO_N8	SDRAM address bus, bit 10		GPIO
170	SD_DQ60	W24	BK3_IO_N19	SDRAM data bus, bit 60		GPIO
171	SD_ADD_R09	T19	BK3_IO_P11	SDRAM address bus, bit 9		GPIO
172	SD_DQ61	Y23	BK3_IO_N24*	SDRAM data bus, bit 61		GPIO
173	SD_ADD_R08	T20	BK3_IO_N11	SDRAM address bus, bit 8		GPIO
174	SD_DQ62	Y22	BK3_IO_P24*	SDRAM data bus, bit 62		GPIO
175	SD_ADD_R07	P19	BK3_IO_P4	SDRAM address bus, bit 7		GPIO
176	SD_DQ63	AA24	BK3_IO_N25*	SDRAM data bus, bit 63		GPIO
177	GND	--	GND	Ground		
178	GND	--	GND			
179	+3.3v	--	VCC_3	Power supply for FPGA IO bank 3		
180	+3.3v	--	VCC_3			
181	+3.3v	--	VCC_3			
182	+3.3v	--	VCC_3			
183	GND	--	GND	Ground		
184	GND	--	GND			
185	SD_ADD_R06	P20	BK3_IO_N4	SDRAM address bus, bit 6		GPIO
186	SD_DQMB3	P21	BK3_IO_P3	SDRAM data mask byte 3		GPIO
187	SD_ADD_R05	P25	BK3_IO_P1	SDRAM address bus, bit 5		GPIO
188	SD_DQMB2	P22	BK3_IO_N3	SDRAM data mask byte 2		GPIO
189	SD_ADD_R04	P26	BK3_IO_N1/VREF	SDRAM address bus, bit 4		GPIO
190	SD_S1#	R22	BK3_IO_N7	SDRAM chip select 1		GPIO
191	SD_ADD_R12	R25	BK3_IO_P5/VREF	SDRAM address bus, bit 12		GPIO
192	SD_S0#	R21	BK3_IO_P7	SDRAM chip select 0		GPIO
193	SD_CAS#	R26	BK3_IO_N5	SDRAM column address strobe		GPIO
194	SD_WE#	R24	BK3_IO_N6	SDRAM write enable		GPIO
195	SD_CKE0	T25	BK3_IO_P9	SDRAM clock enable 0 and 1		GPIO
196	SD_RAS#	T23	BK3_IO_P6	SDRAM row address strobe		GPIO
197	SD_ADD_R03	T26	BK3_IO_N9	SDRAM address bus, bit 3		GPIO
198	SD_DQMB5	U22	BK3_IO_N14	SDRAM data mask byte 5		GPIO
199	SD_ADD_R02	U25	BK3_IO_P12	SDRAM address bus, bit 2		GPIO
200	SD_DQMB4	U21	BK3_IO_P14/VREF	SDRAM data mask byte 4		GPIO
201	SD_ADD_R01	U26	BK3_IO_N12	SDRAM address bus, bit 1		GPIO
202	SD_DQMB0	U20	BK3_IO_N17	SDRAM data mask byte 0		GPIO
203	SD_ADD_R00	V25	BK3_IO_N15	SDRAM address bus, bit 0		GPIO
204	SD_DQMB1	V20	BK3_IO_P17	SDRAM data mask byte 1		GPIO
205	LCD_B0	V24	BK3_IO_P15	LCD data bus, blue bit 0		GPIO
206	LCD_R2	V21	BK3_IO_N20	LCD data bus, red bit 2		GPIO
207	LCD_B1	W26	BK3_IO_N18	LCD data bus, blue bit 1		GPIO
208	LCD_R1	W22	BK3_IO_P20	LCD data bus, red bit 1		GPIO
209	LCD_B2	W25	BK3_IO_P18	LCD data bus, blue bit 2		GPIO
210	LCD_R0	W21	BK3_IO_N22*	LCD data bus, red bit 0		GPIO
211	LCD_B3	Y26	BK3_IO_N21	LCD data bus, blue bit 3		GPIO
212	LCD_G5	W20	BK3_IO_P22*	LCD data bus, green bit 5		GPIO
213	LCD_B4	Y25	BK3_IO_P21	LCD data bus, blue bit 4		GPIO
214	LCD_G4	Y21	BK3_IO_N27*	LCD data bus, green bit 4		GPIO
215	LCD_B5	AA26	BK3_IO_N23*	LCD data bus, blue bit 5		GPIO
216	LCD_DCLK	Y20	BK3_IO_P27*	LCD pixel clock		GPIO
217	LCD_G0	AA25	BK3_IO_P23/VREF*	LCD data bus, green bit 0		GPIO
218	LCD_HSYNC	AA22	BK3_IO_N30/VRP	LCD horizontal sync		GPIO
219	LCD_G1	AB26	BK3_IO_N26*	LCD data bus, green bit 1		GPIO
220	LCD_DTMG	AA21	BK3_IO_P30/VRN	LCD vertical sync		GPIO
221	LCD_G2	AB25	BK3_IO_P26*	LCD data bus, green bit 2		GPIO
222	LCD_R5	AA23	BK3_IO_P25*	LCD data bus, red bit 5		GPIO
223	LCD_G3	AC26	BK3_IO_N28	LCD data bus, green bit 3		GPIO
224	LCD_R4	AB24	BK3_IO_N29/VREF	LCD data bus, red bit 4		GPIO
225	UCB_#RESET	AC25	BK3_IO_P28	UCB touch screen controller reset signal		GPIO
226	LCD_R3	AB23	BK3_IO_P29	LCD data bus, red bit 3		GPIO
227	USB_SYNC	U24	BK3_IO_N13	UCB touch screen controller SYNC signal		GPIO
228	GND	--	GND	Ground		
229	UCB_SDATA_IN	U23	BK3_IO_P13	UCB touch screen controller SDATA_IN		GPIO
230	TDI_U	--	TDI_U	JTAG input data		
231	UCB_BIT_CLK	V22	BK3_IO_P16	UCB touch screen controller BIT_CLK		GPIO
232	TDO_U	--	TDO_U	JTAG output data		
233	UCB_SDATA_OUT	V23	BK3_IO_N16	UCB touch screen controller SDATA_OUT		GPIO

SDRAM module U1-A		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
234	TMS	--	TMS	JTAG select signals	
235	UCB_CLK	W23	BK3_IO_P19/VREF	UCB touch screen controller CLK	GPIO
236	TCK	--	TCK	JTAG clock signal	
237	GND	--	GND	Ground	
238	GND	--	GND		
239	+3.3v	--	+3.3v	+3.3v power supply	
240	+3.3v	--	+3.3v		

The SODIMM 144 socket available in on the SDRAM module can be populated with a standard SDRAM SODIMM 144 with up 512MB of memory. All functional lines from the standard SODIM 144 SDRAM socket are available on the connectors located on the bottom layer (see tables above).

The SODIMM 144 socket is located at position labelled U15. The following figures show the component position on the SDRAM module in which the pin numbers of the connectors are marked.

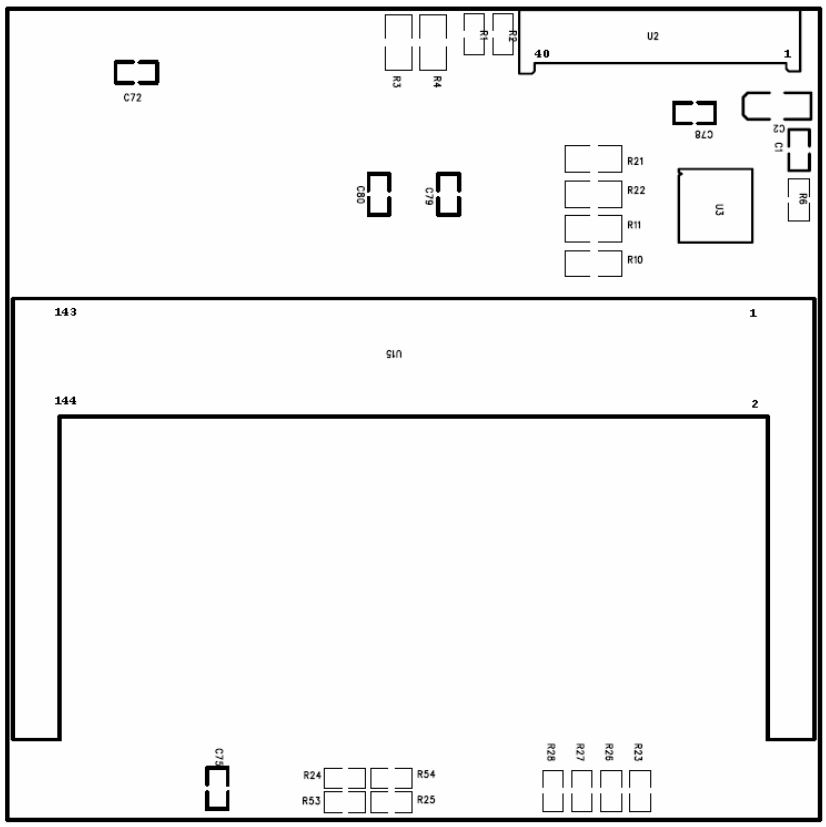

Figure 15. *SDRAM module TOP layer*

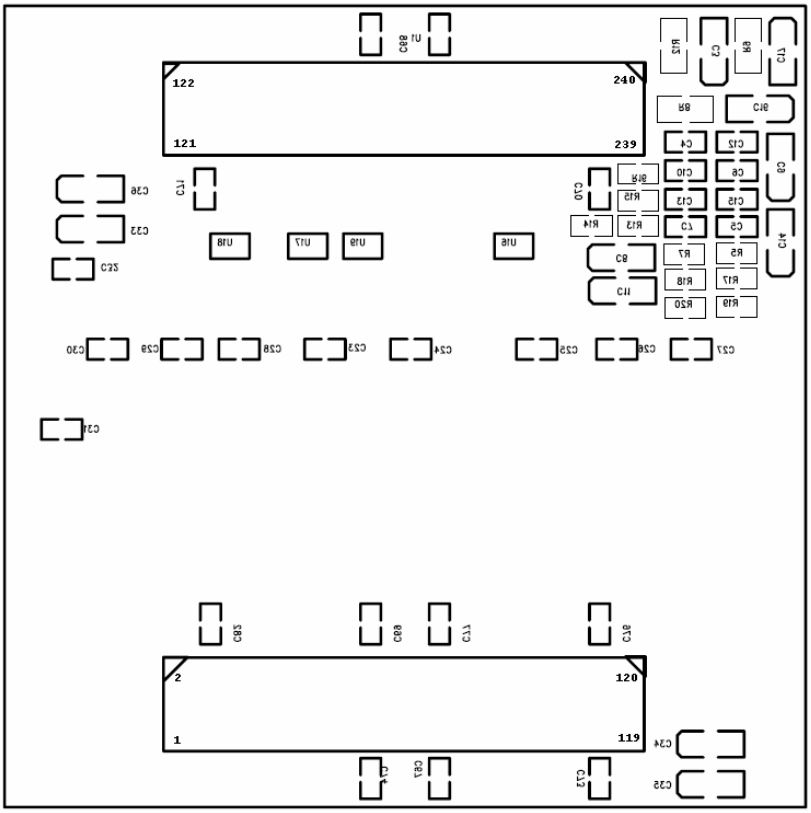

Figure 16. *SDRAM module BOTTOM layer*

The address lines of the SDRAM SO-DIMM can be terminated with serial resistors. These resistors must be populated with the appropriate value when the SDRAM SO-DIMM is intended to be used.

SDRAM module address termination	
SD_ADD[00..03]	U16 populated
SD_ADD[04..07]	U17 populated
SD_ADD[08..13]	U18 populated
SD_ADD[14]	U19 populated

The clock signals can be also terminated. Besides, three different clock configurations can be selected depending on resistor assembly. Next table summarises the possibilities.

SDRAM clock configuration		
Single Clock driven by SD_CK0	R53 - 0R	NO
	R54 – 0R	YES
	R25 – 25R	YES
	R24 – 25R	NO
Single Clock driven by SD_CK1	R53 - 0R	NO
	R54 – 0R	YES
	R25 – 25R	NO
	R24 – 25R	YES
Separated Clocks driven by SD_CK0 and SD_CK1	R53 - 0R	NO
	R54 – 0R	NO
	R25 – 25R	YES
	R24 – 25R	YES
Single Clock driven by SD_CK0, SD_CK1	R53 - 0R	NO
	R54 – 0R	YES

SDRAM clock configuration		
input as return clock for DLL clock adjust	R25 – 25R	YES
	R24 – 0R	YES

Next table enumerates the pin assignment of the SDRAM SO-DIMM where VSS is connected to GND and VDD to +3.3v. The rest are connected to the FPGA module of the system.

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	37	DQ8	73	NC	109	A9
3	DQ0	39	DQ9	75	Vss	111	A10
5	DQ1	41	DQ10	77	NC	113	VDD
7	DQ2	43	DQ11	79	NC	115	DQMB2
9	DQ3	45	VDD	81	VDD	117	DQMB3
11	VDD	47	DQ12	83	DQ16	119	Vss
13	DQ4	49	DQ13	85	DQ17	121	DQ24
15	DQ5	51	DQ14	87	DQ18	123	DQ25
17	DQ6	53	DQ15	89	DQ19	125	DQ26
19	DQ7	55	Vss	91	Vss	127	DQ27
21	Vss	57	NC	93	DQ20	129	VDD
23	DQMB0	59	NC	95	DQ21	131	DQ28
25	DQMB1	61	CK0	97	DQ22	133	DQ29
27	VDD	63	VDD	99	DQ23	135	DQ30
29	A0	65	RAS#	101	VDD	137	DQ31
31	A1	67	WE#	103	A6	139	Vss
33	A2	69	S0#	105	A8	141	SDA
35	Vss	71	S1#	107	Vss	143	VDD

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	Vss	38	DQ40	74	CK1	110	BA1
4	DQ32	40	DQ41	76	Vss	112	A11
6	DQ33	42	DQ42	78	NC	114	VDD
8	DQ34	44	DQ43	80	NC	116	DQMB6
10	DQ35	46	VDD	82	VDD	118	DQMB7
12	VDD	48	DQ44	84	DQ48	120	Vss
14	DQ36	50	DQ45	86	DQ49	122	DQ56
16	DQ37	52	DQ46	88	DQ50	124	DQ57
18	DQ38	54	DQ47	90	DQ51	126	DQ58
20	DQ39	56	Vss	92	Vss	128	DQ59
22	Vss	58	NC	94	DQ52	130	VDD
24	DQMB4	60	NC	96	DQ53	132	DQ60
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
28	VDD	64	VDD	100	DQ55	136	DQ62
30	A3	66	CAS#	102	VDD	138	DQ63
32	A4	68	CKE1	104	A7	140	Vss
34	A5	70	NC/A12[1]	106	BA0	142	SCL
36	Vss	72	NC	108	Vss	144	VDD

NOTE:

1. Pin 70 is No Connect for 256MB modules, or A12 for 512MB modules.

Next table enumerates the lines available on the LCD flat cable labeled U2 located on the top side of the SDRAM module of the system.

Flat Cable U2		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
1	VDD	--	--	+3.3v	
2	VDD	--	--	+3.3v	
3	VDD	--	--	+3.3v	
4	LCD_DCLK	Y20	BK3_IO_P27*	LCD pixel clock signal	GPIO
5	GND	--	--	Ground	
6	LCD_HSYNC	AA22	BK3_IO_N30/VRP	LCD horizontal sync signal	GPIO
7	GND	--	--	Ground	
8	LCD_DTMG	AA21	BK3_IO_P30/VRN	LCD vertical sync signal	GPIO
9	GND	--	--	Ground	
10	NC	--	--	Not connected	
11	GND	--	--	Ground	
12	LCD_R5	AA23	BK3_IO_P25*	LCD Red bit 5	GPIO
13	LCD_R4	AB24	BK3_IO_N29/VREF	LCD Red bit 4	GPIO
14	LCD_R3	AB23	BK3_IO_P29	LCD Red bit 3	GPIO
15	GND	--	--	Ground	
16	LCD_R2	V21	BK3_IO_N20	LCD Red bit 2	GPIO
17	LCD_R1	W22	BK3_IO_P20	LCD Red bit 1	GPIO
18	LCD_R0	W21	BK3_IO_N22*	LCD Red bit 0	GPIO
19	GND	--	--	Ground	
20	LCD_G5	W20	BK3_IO_P22*	LCD Green bit 5	GPIO
21	LCD_G4	Y21	BK3_IO_N27*	LCD Green bit 4	GPIO
22	LCD_G3	AC26	BK3_IO_N28	LCD Green bit 3	GPIO
23	GND	--	--	Ground	
24	LCD_G2	AB25	BK3_IO_P26*	LCD Green bit 2	GPIO
25	LCD_G1	AB26	BK3_IO_N26*	LCD Green bit 1	GPIO
26	LCD_G0	AA25	BK3_IO_P23/VREF*	LCD Green bit 0	GPIO
27	GND	--	--	Ground	
28	LCD_B5	AA26	BK3_IO_N23*	LCD Blue bit 5	GPIO
29	LCD_B4	Y25	BK3_IO_P21	LCD Blue bit 4	GPIO
30	LCD_B3	Y26	BK3_IO_N21	LCD Blue bit 3	GPIO

Flat Cable U2		FPGA		Description	
Pin	NAME	Pin	Name	System	FPGA module
31	GND	--	--	Ground	
32	LCD_B2	W25	BK3_IO_P18	LCD Blue bit 2	GPIO
33	LCD_B1	W26	BK3_IO_N18	LCD Blue bit 1	GPIO
34	LCD_B0	V24	BK3_IO_P15	LCD Blue bit 0	GPIO
35	PCI	--	--	LCD ref voltage	--
36	VCNTRL	--	--	LCD voltage control	--
37	LCD_XR	--	--	Touch screen analog line	--
38	LCD_YL	--	--	Touch screen analog line	--
39	LCD_XL	--	--	Touch screen analog line	--
40	LCD_YU	--	--	Touch screen analog line	--


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