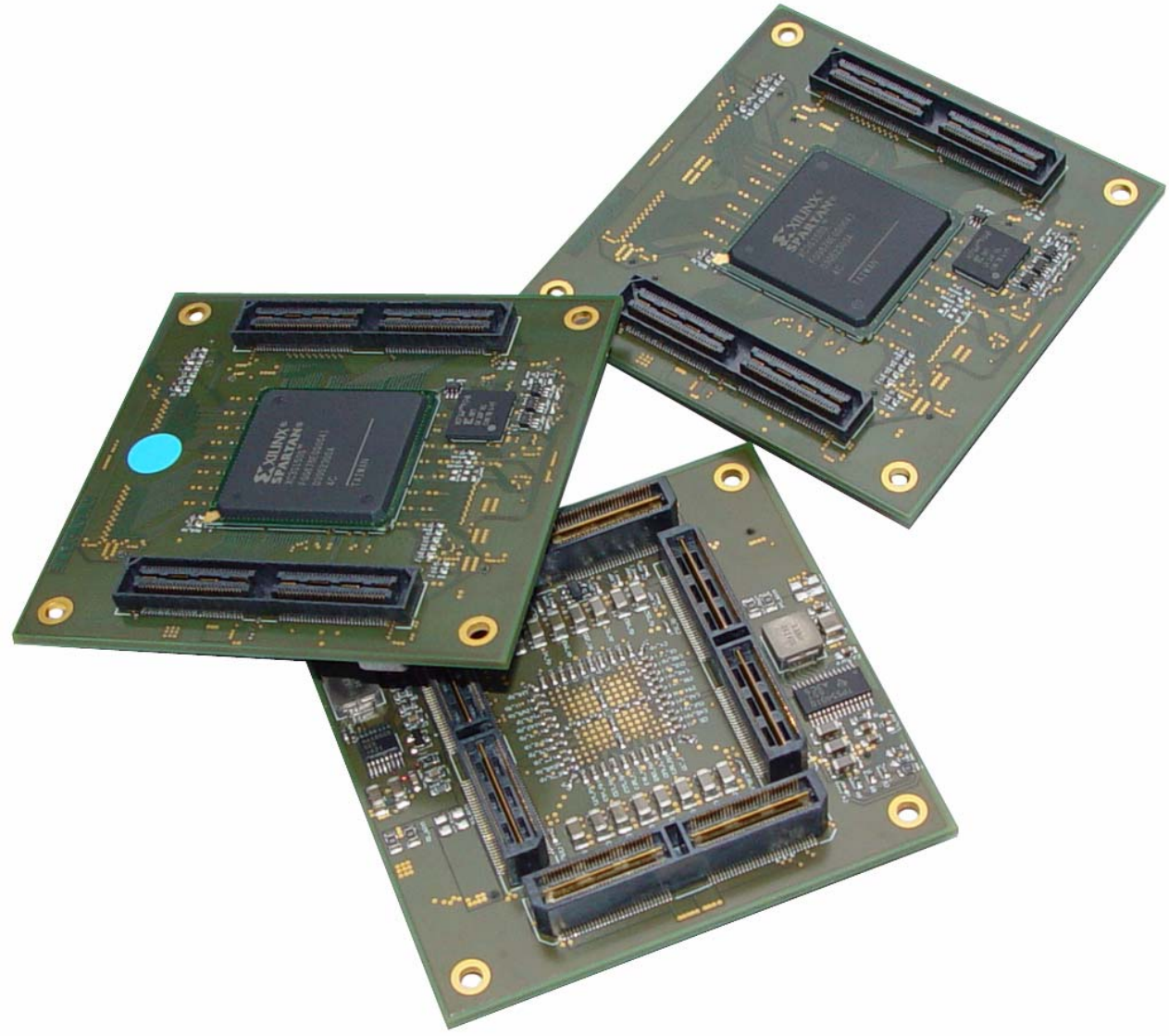
ERIZOV0-XC3S1500
Hardware manual



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1 Features and architecture

The ramDSP Electronics ERIZOV0-XC3S1500 is a 70x70mm stackable FPGA module that gathers the following resources:

- XILINX SPARTAN-III XC3S1500-4FG676C FPGA.
- XILINX XCF16PFSG48C configuration PROM.
- ABRACOM 50MHz crystal oscillator ASD-50.0-E-R-50 (not populated).
- A Texas Instruments TPS54010PWP switching DCDC converter configured to generate 1.2v used as FPGA core voltage.
- A MAXIM MAX8505EEE switching DCDC converter configured to generate 2.5v used as auxiliary FPGA voltage (VCCAUX) and alternative FPGA banks power supply.
- A Texas Instruments TPS72218DBV linear voltage regulator configured to generate 1.8v supplying the core voltage of the XILINX configuration PROM.
- 4 different Texas Instruments SN74LVC1G126DCK used as level shifters that make the FPGA Module fully 3.3v tolerant and configuration bus multiplexer.
- 4 high speed SAMTEC QTH-060-02-L-D-A connectors on the bottom layer and 2 SAMTEC QSH-060-02-L-D-A connectors on the top layer.
- 486 IO's available on module connectors.

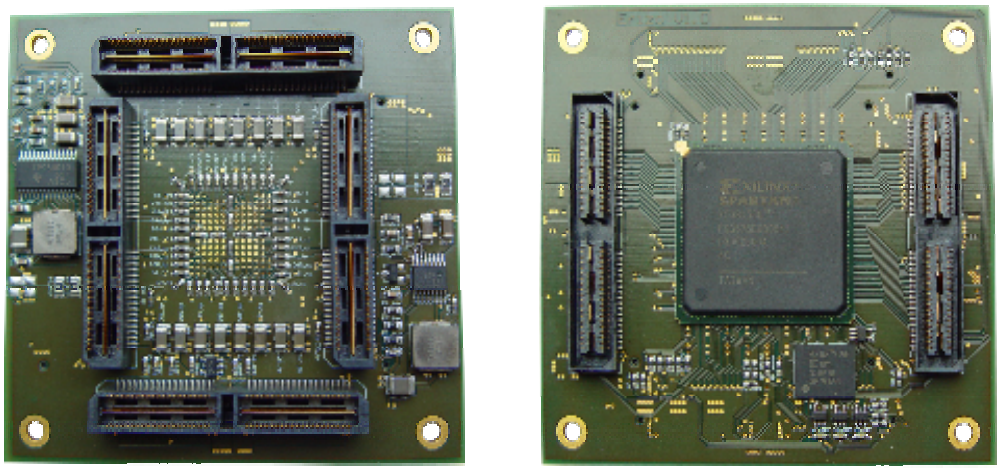


Figure 1. *Top and bottom view of ERIZOV0-XC3S1500 FPGA module*

The FPGA module architecture is shown in the following block diagram.

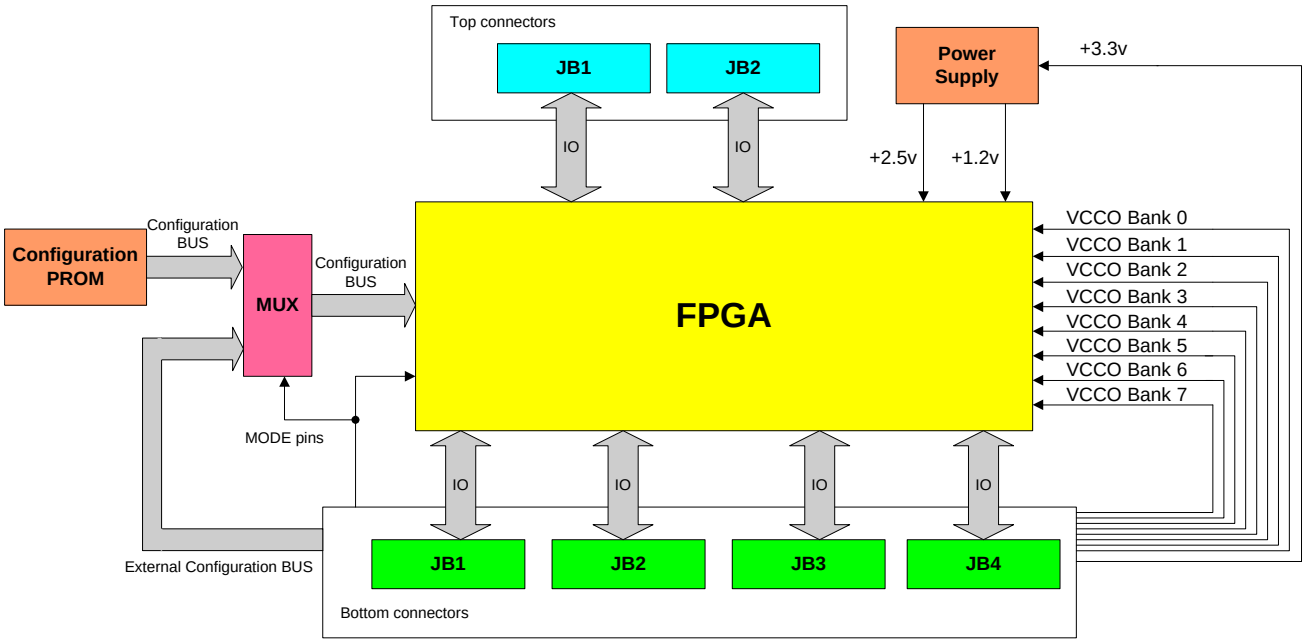


Figure 2. *ERIZOV0-XC3S1500 FPGA module architecture*

1.1 Configuration modes

The configuration mode of the FPGA can be selected using the MODE signals (M0, M1 and M2) which are available in the FPGA module connectors. Next table summarises the configuration possibilities:

Mode	M0	M1	M2	Description
Master Serial	0	0	0	Supported. Configuration is loaded from PROM (default set by pull-down resistors).
Slave Serial	1	1	1	Supported. The Configuration is loaded externally.
Master Parallel	*1*	*1*	*0*	*Not supported.*
Slave Parallel	0	1	1	Supported. The Configuration is loaded externally.
JTAG	1	0	1	The FPGA is programmed through JTAG port

1.2 Power Supply

The ERIZOV0-XC3S1500 module can be powered from a single power supply of +3.3v. Alternatively each FPGA IO bank can be powered independently with different voltages.

Next table describes the power nets available in the module connectors.

Power Supply net at connector	Description	Number of lines
+3.3V	Main power line feeds FPGA core and auxiliary voltage regulators	16
VCCO_0	FPGA IO bank 0 power supply	2
VCCO_1	FPGA IO bank 1 power supply	2
VCCO_2	FPGA IO bank 2 power supply	2
VCCO_3	FPGA IO bank 3 power supply. Internally can be assigned to +2.5v or 3.3v.	2
VCCO_4	FPGA IO bank 4 power supply	2
VCCO_5	FPGA IO bank 5 power supply	2
VCCO_6	FPGA IO bank 6 power supply	2
VCCO_7	FPGA IO bank 7 power supply. Internally can be assigned to +2.5v or 3.3v.	2
GND	ground connection	33 + 4 SHIELDS

The power supply scheme of the FPGA module is sketched in the following figure.

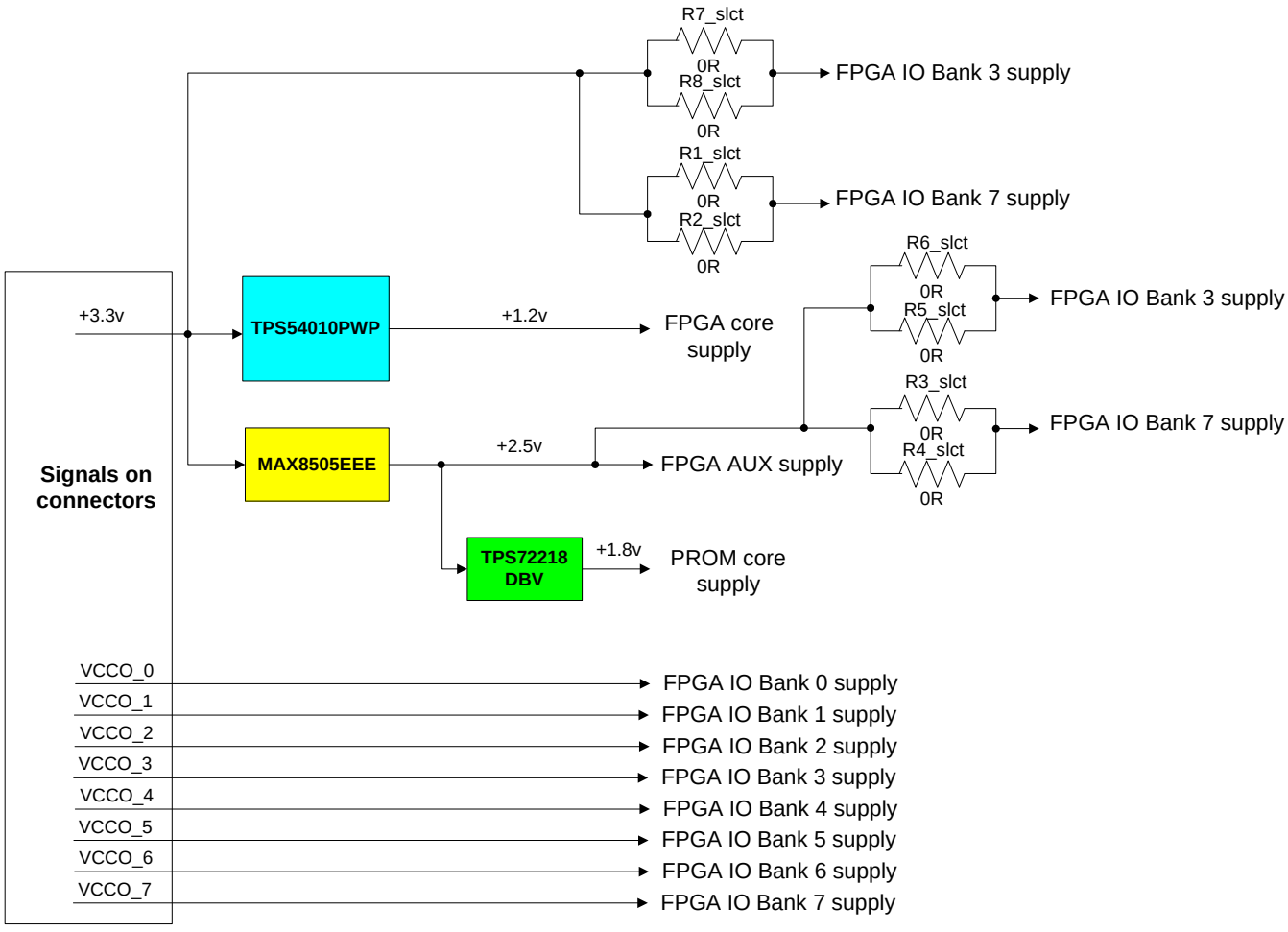


Figure 3. *ERIZOV0-XC3S1500 FPGA module power supply scheme*

A set of resistors allows selecting the source of power for FPGA IO banks 3 and 7. Next tables enumerate all possible configurations. Refer to figure 10 and 11 for resistor location.

VCCO BANK 3		
External power supply	R8_slct	Not populated
	R7_slct	Not populated
	R6_slct	Not populated
	R5_slct	Not populated
Internal +3.3v	R8_slct	populated
	R7_slct	populated
	R6_slct	Not populated
	R5_slct	Not populated
Internal +2.5v	R8_slct	Not populated
	R7_slct	Not populated
	R6_slct	Populated
	R5_slct	Populated

VCCO BANK 7		
External power supply	R1_slct	Not populated
	R2_slct	Not populated
	R3_slct	Not populated
	R4_slct	Not populated
Internal +3.3v	R1_slct	populated
	R2_slct	populated
	R3_slct	Not populated
	R4_slct	Not populated
Internal +2.5v	R1_slct	Not populated
	R2_slct	Not populated
	R3_slct	Populated
	R4_slct	Populated

1.3 JTAG chain

A set of zero ohm resistors allows selecting different JTAG chain configurations. Figure below shows three supported JTAG chain configurations.

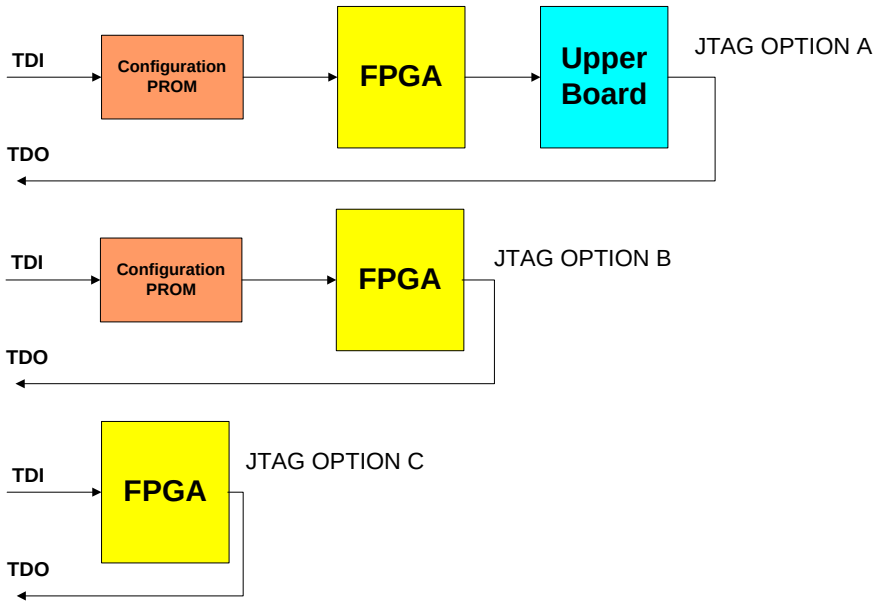


Figure 4. *ERIZOV0-XC3S1500 FPGA module JTAG chain options*

Next tables summarise the resistor set possibilities for all JTAG chain configurations. Refer to figures 10 and 11 for resistor location.

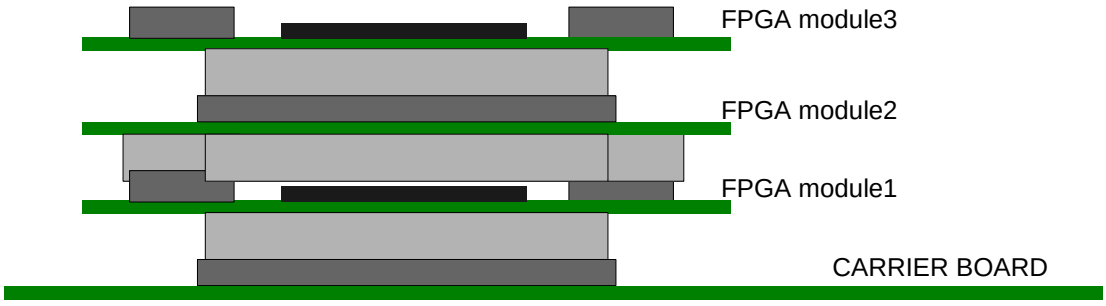
JTAG OPTION A		
PROM + FPGA + UPPER Board	R8_JT	populated
	R6_JT	Not populated
	R7_JT	populated
	R5_JT	Not populated
	R4_JT	populated

JTAG OPTION B		
PROM + FPGA	R8_JT	populated
	R6_JT	Not populated
	R7_JT	Not populated
	R5_JT	populated
	R4_JT	Not populated

JTAG OPTION C		
FPGA	R8_JT	Not populated
	R6_JT	populated
	R7_JT	Not populated
	R5_JT	populated
	R4_JT	Not populated

1.4 FPGA module stacking

In case of stacking several FPGA modules, the power supply and number of available FPGA IO banks are limited for the upper FPGA modules.



CONNECTOR	POWER LINES				GPIO	PLUGGABLE TO
JB1	3.3v → 4 lines	VCCO0 → 2 lines	VCCO1 → 2 lines	GND → 9 lines + SHIELD	99 lines	JT2
JB2	3.3v → 4 lines	VCCO2 → 2 lines	VCCO3 → 2 lines	GND → 8 lines + SHIELD	81 lines	
JB3	3.3v → 4 lines	VCCO4 → 2 lines	VCCO5 → 2 lines	GND → 8 lines + SHIELD	97 lines	JT1
JB4	3.3v → 4 lines	VCCO6 → 2 lines	VCCO7 → 2 lines	GND → 8 lines + SHIELD	85 lines	
JT2	3.3v → 4 lines	VCCO3 → 4 lines		GND → 9 lines + SHIELD	60 lines	JB1
JT1	3.3v → 4 lines	VCCO7 → 4 lines		GND → 8 lines + SHIELD	64 lines	JB3

Figure 5. *ERIZOV0-XC3S1500 FPGA module stacking example*

The current consumed by the upper FPGA's (FPGA module 2 and 3) is delivered through the connectors JT1 and JT2 of the top layer of the first FPGA in the stack. Connector JT1 powers IO Bank4, IO Bank5 and +3.3V nets and controls the configuration bus of the next FPGA. Connector JT2 powers IO Bank0, IO Bank1 and +3.3V nets and controls the JTAG port of the next FPGA. On the upper FPGA (FPGA module 2 and 3) Bank 3 and Bank 7 can be internally powered by +3.3v, but IO Bank 2 and IO Bank 6 are left unconnected. The IO lines belonging to IO Bank 2 and IO Bank 6 in connectors JB2 and JB4 are unconnected too.

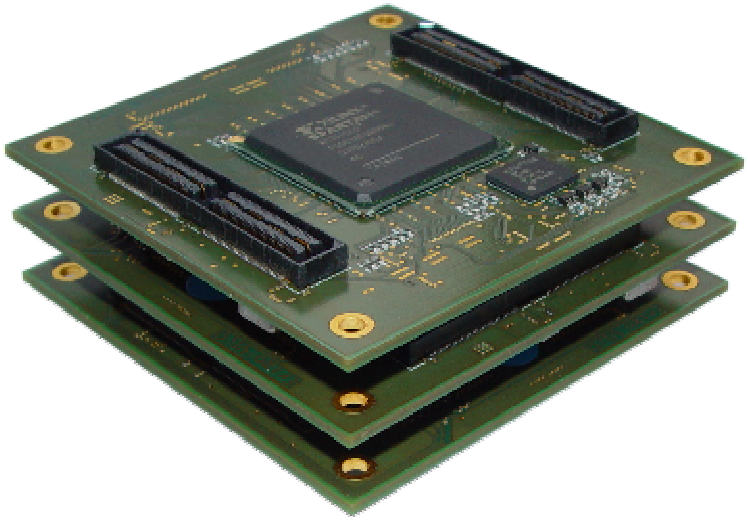


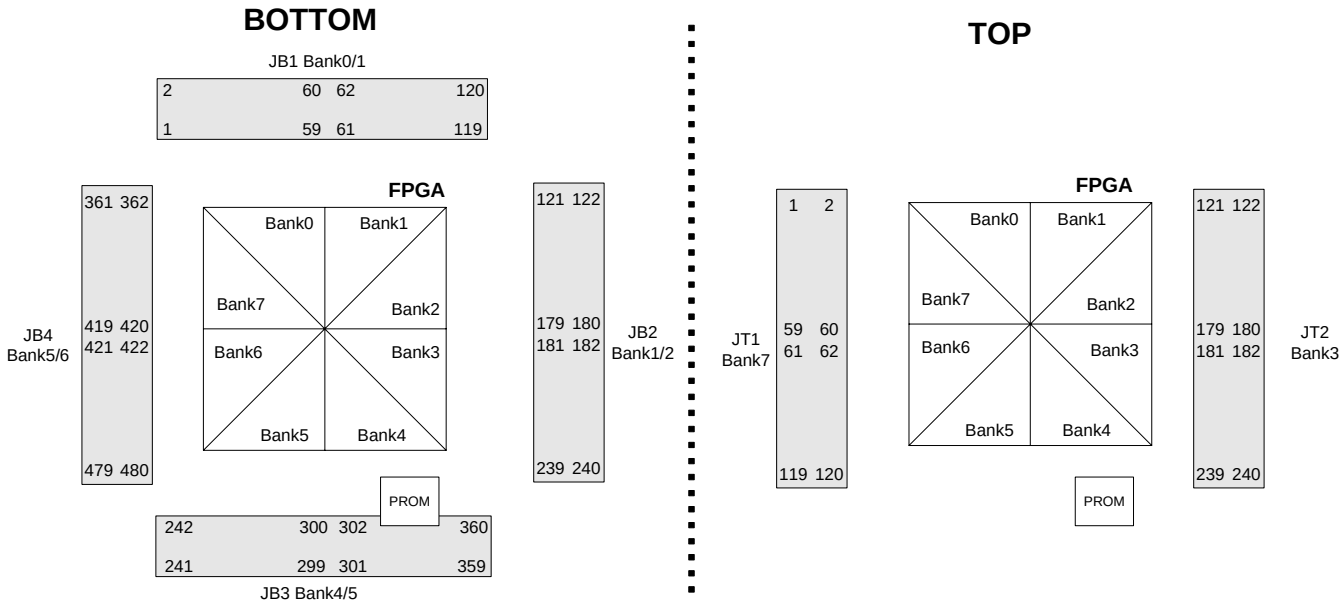
Figure 6. *ERIZOV0-XC3S1500 FPGA module stacking example*

1.5 Technical characteristics

Technical characteristics		
+3.3v net typical voltage	+3.3v	Sources FPGA VCCINT and VCCAUX
+3.3v net minimum current	200mA	
+3.3v net max current	--	FPGA/HDL design dependent
VCCO nets typical voltage	1.8v,2.5v,+3.3v	More details on Xilinx Spartan-III datasheet
VCCO minimum/max current	--	FPGA/HDL design dependent
Size in mm	70 x 70	
Operating Temperature	0°-+70°	

2 Module connectors pin assignment

Next figure shows the position of the connectors on the bottom and top sides of the FPGA module indicating the pin numbering.



CONNECTOR	POWER LINES				GPIO	PLUGGABLE TO
JB1	3.3v → 4 lines	VCCO0 → 2 lines	VCCO1 → 2 lines	GND → 9 lines + SHIELD	99 lines	JT2
JB2	3.3v → 4 lines	VCCO2 → 2 lines	VCCO3 → 2 lines	GND → 8 lines + SHIELD	81 lines	
JB3	3.3v → 4 lines	VCCO4 → 2 lines	VCCO5 → 2 lines	GND → 8 lines + SHIELD	97 lines	JT1
JB4	3.3v → 4 lines	VCCO6 → 2 lines	VCCO7 → 2 lines	GND → 8 lines + SHIELD	85 lines	
JT2	3.3v → 4 lines	VCCO3 → 4 lines		GND → 9 lines + SHIELD	60 lines	JB1
JT1	3.3v → 4 lines	VCCO7 → 4 lines		GND → 8 lines + SHIELD	64 lines	JB3

Figure 7. *ERIZOV0-XC3S1500 FPGA module pin locations and quantitative description*

Module Connectors	Connector Type
JB1	SAMTEC QTH-060-02-L-D-A
JB2	SAMTEC QTH-060-02-L-D-A
JB3	SAMTEC QTH-060-02-L-D-A
JB4	SAMTEC QTH-060-02-L-D-A
JT1	SAMTEC QSH-060-02-L-D-A
JT2	SAMTEC QSH-060-02-L-D-A

2.1 Bottom connectors

The connectors JB1, JB2, JB3 and JB4 located on the bottom layer are SAMTEC QTH-060-02-L-D-A that mate to SAMTEC QSH-060-02-L-D-A (placed on carrier board).

Next tables enumerate the pin assignment of the bottom connectors on the FPGA module.

Connector JB1	FPGA		Description	
Pin	Pin	Name	System	module
1	--	+3.3v	+3.3v power supply	
2	--	+3.3v		
3	--	GND	Ground	
4	--	GND		
5	E5	BK0_IO_N25/VRP	T.B.D.	GPIO/ Bank 0 VRP
6	B3	BK0_IO_S12/VREF	T.B.D.	GPIO/ Bank 0 VREF
7	D5	BK0_IO_P25/VRN	T.B.D.	GPIO/ Bank 0 VRN
8	A3	BK0_IO_S11	T.B.D.	GPIO
9	C5	BK0_IO_N23	T.B.D.	GPIO
10	C4	BK0_IO_S10	T.B.D.	GPIO
11	B5	BK0_IO_P23	T.B.D.	GPIO
12	A4	BK0_IO_P24/VREF	T.B.D.	GPIO/ Bank 0 VREF
13	C6	BK0_IO_N21	T.B.D.	GPIO
14	B4	BK0_IO_N24	T.B.D.	GPIO
15	B6	BK0_IO_P21	T.B.D.	GPIO
16	A5	BK0_IO_S9	T.B.D.	GPIO
17	E7	BK0_IO_N20	T.B.D.	GPIO
18	C8	BK0_IO_S6*	T.B.D.	GPIO
19	D7	BK0_IO_P20	T.B.D.	GPIO
20	A6	BK0_IO_S8	T.B.D.	GPIO
21	E6	BK0_IO_N22	T.B.D.	GPIO
22	B7	BK0_IO_N19	T.B.D.	GPIO
23	D6	BK0_IO_P22	T.B.D.	GPIO
24	A7	BK0_IO_P19	T.B.D.	GPIO
25	F7	BK0_IO_S7/VREF	T.B.D.	GPIO/ Bank 0 VREF
26	B8	BK0_IO_N16	T.B.D.	GPIO
27	E8	BK0_IO_N17*	T.B.D.	GPIO
28	A8	BK0_IO_P16	T.B.D.	GPIO
29	D8	BK0_IO_P17*	T.B.D.	GPIO
30	C12	BK0_IO_S2	T.B.D.	GPIO
31	G8	BK0_IO_N18*	T.B.D.	GPIO
32	B10	BK0_IO_N10*	T.B.D.	GPIO
33	F8	BK0_IO_P18*	T.B.D.	GPIO
34	A10	BK0_IO_P10*	T.B.D.	GPIO
35	E9	BK0_IO_N14*	T.B.D.	GPIO
36	B11	BK0_IO_N7*	T.B.D.	GPIO
37	D9	BK0_IO_P14*	T.B.D.	GPIO
38	A11	BK0_IO_P7/VREF*	T.B.D.	GPIO/ Bank 0 VREF
39	C9	BK0_IO_N13*	T.B.D.	GPIO
40	B12	BK0_IO_N4	T.B.D.	GPIO
41	B9	BK0_IO_P13*	T.B.D.	GPIO
42	A12	BK0_IO_P4	T.B.D.	GPIO
43	G9	BK0_IO_N15	T.B.D.	GPIO
44	B13	BK0_IO_N1/CLK7	T.B.D.	GPIO/GCLK
45	F9	BK0_IO_P15	T.B.D.	GPIO
46	A13	BK0_IO_P1/CLK6	T.B.D.	GPIO/GCLK
47	G10	BK0_IO_S5/VREF	T.B.D.	GPIO/ Bank 0 VREF
48	D11	BK0_IO_P8	T.B.D.	GPIO
49	F10	BK0_IO_N12	T.B.D.	GPIO
50	E11	BK0_IO_N8	T.B.D.	GPIO
51	E10	BK0_IO_P12	T.B.D.	GPIO
52	G11	BK0_IO_N9	T.B.D.	GPIO
53	D10	BK0_IO_N11	T.B.D.	GPIO
54	F11	BK0_IO_P9	T.B.D.	GPIO
55	C10	BK0_IO_P11	T.B.D.	GPIO
56	H12	BK0_IO_S3	T.B.D.	GPIO
57	--	GND	Ground	
58	--	GND		
59	--	VCC_0	Power supply for FPGA IO bank 0 and bank 1	
60	--	VCC_0		
61	--	VCC_1		
62	--	VCC_1		
63	--	GND	Ground	
64	--	GND		
65	H11	BK0_IO_S4	T.B.D.	GPIO
66	E13	BK0_IO_S1	T.B.D.	GPIO
67	G12	BK0_IO_N6	T.B.D.	GPIO
68	C13	BK0_IO_P2/VREF	T.B.D.	GPIO/ Bank 0 VREF
69	H13	BK0_IO_P6	T.B.D.	GPIO

Connector JB1	FPGA		Description	
Pin	Pin	Name	System	module
70	D13	BK0_IO_N2	T.B.D.	GPIO
71	H14	BK1_IO_P3	T.B.D.	GPIO
72	C15	BK1_IO_S3/VREF	T.B.D.	GPIO/ Bank 1 VREF
73	G14	BK1_IO_N3	T.B.D.	GPIO
74	A14	BK1_IO_S1	T.B.D.	GPIO
75	F12	BK0_IO_N5	T.B.D.	GPIO
76	B15	BK1_IO_P4	T.B.D.	GPIO
77	E12	BK0_IO_P5	T.B.D.	GPIO
78	A15	BK1_IO_N4	T.B.D.	GPIO
79	F13	BK0_IO_P3	T.B.D.	GPIO
80	B16	BK1_IO_P7*	T.B.D.	GPIO
81	G13	BK0_IO_N3	T.B.D.	GPIO
82	A16	BK1_IO_N7*	T.B.D.	GPIO
83	F14	BK1_IO_S2	T.B.D.	GPIO
84	B17	BK1_IO_P10*	T.B.D.	GPIO
85	D14	BK1_IO_N2/VREF	T.B.D.	GPIO/ Bank 1 VREF
86	A17	BK1_IO_N10*	T.B.D.	GPIO
87	E14	BK1_IO_P2	T.B.D.	GPIO
88	C17	BK1_IO_S5/VREF	T.B.D.	GPIO/ Bank 1 VREF
89	F15	BK1_IO_P5	T.B.D.	GPIO
90	B19	BK1_IO_P15	T.B.D.	GPIO
91	E15	BK1_IO_N5	T.B.D.	GPIO
92	A19	BK1_IO_N15	T.B.D.	GPIO
93	G16	BK1_IO_N9	T.B.D.	GPIO
94	B20	BK1_IO_P18	T.B.D.	GPIO
95	H16	BK1_IO_P9	T.B.D.	GPIO
96	A20	BK1_IO_N18/VREF	T.B.D.	GPIO/ Bank 1 VREF
97	F17	BK1_IO_N12	T.B.D.	GPIO
98	B21	BK1_IO_P20	T.B.D.	GPIO
99	G17	BK1_IO_P12	T.B.D.	GPIO
100	A21	BK1_IO_N20	T.B.D.	GPIO
101	F18	BK1_IO_N14	T.B.D.	GPIO
102	A22	BK1_IO_S10	T.B.D.	GPIO
103	G18	BK1_IO_P14	T.B.D.	GPIO
104	D18	BK1_IO_S6/VREF*	T.B.D.	GPIO/ Bank 1 VREF
105	F19	BK1_IO_P17*	T.B.D.	GPIO
106	A23	BK1_IO_S11	T.B.D.	GPIO
107	E19	BK1_IO_N17*	T.B.D.	GPIO
108	--	GND	Ground	
109	G19	BK1_IO_S8	T.B.D.	GPIO
110	--	TDI	JTAG data input	
111	F20	BK1_IO_S9	T.B.D.	GPIO
112	--	TDO	JTAG data output	
113	F21	BK1_IO_P23	T.B.D.	GPIO
114	--	TMS	JTAG chip select	
115	E21	BK1_IO_N23	T.B.D.	GPIO
116	--	TCK	JTAG clock signal	
117	--	GND	Ground	
118	--	GND		
119	--	+3.3v	+3.3v power supply	
120	--	+3.3v		

Connector JB2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
121	--	+3.3v	+3.3v power supply	
122	--	+3.3v		
123	--	GND	Ground	
124	--	GND		
125	C18	BK1_IO_P13*	T.B.D.	GPIO
126	G15	BK1_IO_N6	T.B.D.	GPIO
127	B18	BK1_IO_N13*	T.B.D.	GPIO
128	H15	BK1_IO_P6	T.B.D.	GPIO
129	D19	BK1_IO_P16*	T.B.D.	GPIO
130	F16	BK1_IO_P8	T.B.D.	GPIO
131	C19	BK1_IO_N16*	T.B.D.	GPIO
132	E16	BK1_IO_N8	T.B.D.	GPIO

Connector JB2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
133	D20	BK1_IO_N19	T.B.D.	GPIO
134	D16	BK1_IO_S4	T.B.D.	GPIO
135	E20	BK1_IO_P19	T.B.D.	GPIO
136	D17	BK1_IO_N11	T.B.D.	GPIO
137	C21	BK1_IO_N21	T.B.D.	GPIO
138	E17	BK1_IO_P11	T.B.D.	GPIO
139	D21	BK1_IO_P21	T.B.D.	GPIO
140	E18	BK1_IO_S7	T.B.D.	GPIO
141	B22	BK1_IO_N22/VREF	T.B.D.	GPIO/ Bank 1 VREF
142	C25	BK2_IO_N1/VRP	T.B.D.	GPIO/ Bank 2 VRP
143	C22	BK1_IO_P22	T.B.D.	GPIO
144	C26	BK2_IO_P1/VRN	T.B.D.	GPIO/ Bank 2 VRN
145	B23	BK1_IO_N24	T.B.D.	GPIO
146	D25	BK2_IO_N3/VREF	T.B.D.	GPIO/ Bank 2 VREF
147	C23	BK1_IO_P24	T.B.D.	GPIO
148	D26	BK2_IO_P3	T.B.D.	GPIO
149	D22	BK1_IO_N25/VRP	T.B.D.	GPIO/ Bank 1 VRP
150	E25	BK2_IO_N4*	T.B.D.	GPIO
151	E22	BK1_IO_P25/VRN	T.B.D.	GPIO/ Bank 1 VRN
152	E26	BK2_IO_P4*	T.B.D.	GPIO
153	E23	BK2_IO_N2	T.B.D.	GPIO
154	F25	BK2_IO_N8/VREF*	T.B.D.	GPIO/ Bank 2 VREF
155	E24	BK2_IO_P2	T.B.D.	GPIO
156	F26	BK2_IO_P8*	T.B.D.	GPIO
157	F23	BK2_IO_N6*	T.B.D.	GPIO
158	G25	BK2_IO_N9*	T.B.D.	GPIO
159	F24	BK2_IO_P6*	T.B.D.	GPIO
160	G26	BK2_IO_P9*	T.B.D.	GPIO
161	K20	BK2_IO_P14	T.B.D.	GPIO
162	H25	BK2_IO_N13	T.B.D.	GPIO
163	J20	BK2_IO_N14	T.B.D.	GPIO
164	H26	BK2_IO_P13	T.B.D.	GPIO
165	J22	BK2_IO_N15	T.B.D.	GPIO
166	K25	BK2_IO_N19	T.B.D.	GPIO
167	J23	BK2_IO_P15	T.B.D.	GPIO
168	K26	BK2_IO_P19	T.B.D.	GPIO
169	K21	BK2_IO_N17/VREF	T.B.D.	GPIO/ Bank 2 VREF
170	L25	BK2_IO_N22	T.B.D.	GPIO
171	K22	BK2_IO_P17	T.B.D.	GPIO
172	L26	BK2_IO_P22	T.B.D.	GPIO
173	L21	BK2_IO_N21	T.B.D.	GPIO
174	M25	BK2_IO_N26/VREF	T.B.D.	GPIO/ Bank 2 VREF
175	L22	BK2_IO_P21	T.B.D.	GPIO
176	M26	BK2_IO_P26	T.B.D.	GPIO
177	--	GND	Ground	
178	--	GND		
179	--	VCC_2	Power supply for FPGA IO bank 2 and bank.	
180	--	VCC_2		
181	--	VCC_3	Power supply for FPGA IO bank 3 can be taken from internal 2.5V, internal 3.3V, external JB2 or external JT2.	
182	--	VCC_3		
183	--	GND	Ground	
184	--	GND		
185	N22	BK2_IO_P28	T.B.D.	GPIO
186	N25	BK2_IO_N30	T.B.D.	GPIO
187	N21	BK2_IO_N28	T.B.D.	GPIO
188	N26	BK2_IO_P30/VREF	T.B.D.	GPIO/ Bank 2 VREF
189	K24	BK2_IO_P18	T.B.D.	GPIO
190	G20	BK2_IO_N5*	T.B.D.	GPIO
191	K23	BK2_IO_N18	T.B.D.	GPIO
192	G21	BK2_IO_P5*	T.B.D.	GPIO
193	M19	BK2_IO_N23	T.B.D.	GPIO
194	**F22**	**BK2_IO_S1****	**Not present in XC3S1500**	**GPIO**
195	M20	BK2_IO_P23	T.B.D.	GPIO
196	H20	BK2_IO_N10	T.B.D.	GPIO
197	N20	BK2_IO_P27	T.B.D.	GPIO
198	H21	BK2_IO_P10	T.B.D.	GPIO
199	N19	BK2_IO_N27	T.B.D.	GPIO
200	J21	BK2_IO_P11	T.B.D.	GPIO
201	M22	BK2_IO_P24	T.B.D.	GPIO

Connector JB2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
202	H22	BK2_IO_N11	T.B.D.	GPIO
203	M21	BK2_IO_N24	T.B.D.	GPIO
204	G22	BK2_IO_N7*	T.B.D.	GPIO
205	L20	BK2_IO_P20	T.B.D.	GPIO
206	G23	BK2_IO_P7*	T.B.D.	GPIO
207	L19	BK2_IO_N20	T.B.D.	GPIO
208	H24	BK2_IO_P12/VREF	T.B.D.	GPIO/ Bank 2 VREF
209	--	NC	Not connected	
210	H23	BK2_IO_N12	T.B.D.	GPIO
211	--	NC	Not connected	
212	J24	BK2_IO_N16	T.B.D.	GPIO
213	--	NC	Not connected	
214	J25	BK2_IO_P16	T.B.D.	GPIO
215	--	NC	Not connected	
216	M24	BK2_IO_P25	T.B.D.	GPIO
217	--	NC	Not connected	
218	L23	BK2_IO_N25	T.B.D.	GPIO
219	--	NC	Not connected	
220	N24	BK2_IO_P29	T.B.D.	GPIO
221	--	NC	Not connected	
222	**N23**	**BK2_IO_N29**	**Not present in XC3S1500**	**GPIO**
223	--	NC	Not connected	
224	--	NC	Not connected	
225	--	NC	Not connected	
226	--	NC	Not connected	
227	--	NC	Not connected	
228	--	NC	Not connected	
229	--	NC	Not connected	
230	--	NC	Not connected	
231	--	NC	Not connected	
232	--	NC	Not connected	
233	--	NC	Not connected	
234	--	NC	Not connected	
235	--	NC	Not connected	
236	--	NC	Not connected	
237	--	GND	Ground	
238	--	GND		
239	--	+3.3v	+3.3v power supply	
240	--	+3.3v		

Connector JB3	FPGA		Description	
Pin	Pin	Name	System	FPGA module
241	--	+3.3v	+3.3v power supply	
242	--	+3.3v		
243	--	GND	Ground	
244	--	GND		
245	Y15	BK4_IO_N6/**D0_C**	configuration bus bit 0	GPI (only input to the system when M2 is high)
246	--	**M0**		Configuration Mode selection bit 0
247	W14	BK4_IO_P6/**D1**	configuration bus bit 1	GPIO
248	--	**M1**		Configuration Mode selection bit 1
249	Y14	BK4_IO_N3/**D2**	configuration bus bit 2	GPIO
250	--	**M2**		Configuration Mode selection bit 2
251	AA14	BK4_IO_P3/**D3**	configuration bus bit 3	GPIO
252	AD14	BK4_IO_P2/**DOUT**	configuration data output for daisy chain	GPIO
253	AC13	BK5_IO_N2/**D4**	configuration bus bit 4	GPIO
254	AC14	BK4_IO_N2/**INITB**	INITB configuration control line	GPIO
255	AB13	BK5_IO_P2/**D5**	configuration bus bit 5	GPIO
256	AC5	BK5_IO_N25/**RDWR_B**	RDWR_B configuration control line	GPIO
257	AB12	BK5_IO_N5/**D6**	configuration bus bit 6	GPIO
258	AB5	BK5_IO_P25/**CS_B**	CS_B configuration	GPIO

Connector JB3	FPGA		Description	
Pin	Pin	Name	System	FPGA module
			control line	
259	AA12	BK5_IO_P5/**D7**	configuration bus bit 7	GPIO
260	--	**PROG_B**		Resets FPGA configuration
261	AB10	BK5_IO_P11	T.B.D.	GPIO
262	--	**CCLK**		Configuration cock
263	AC10	BK5_IO_N11	T.B.D.	GPIO
264	--	**DONE_G**		DONE_G configuration control line
265	W11	BK5_IO_P9	T.B.D.	GPIO
266	AF5	BK5_IO_S10/VREF	T.B.D.	GPIO/ Bank 5 VREF
267	Y11	BK5_IO_N9	T.B.D.	GPIO
268	AE6	BK5_IO_P20	T.B.D.	GPIO
269	AD10	BK5_IO_S5	T.B.D.	GPIO
270	AF6	BK5_IO_N20	T.B.D.	GPIO
271	AC11	BK5_IO_S4	T.B.D.	GPIO
272	AE7	BK5_IO_P18/VRN	T.B.D.	GPIO/ Bank 5 VRN
273	Y12	BK5_IO_N6/VREF	T.B.D.	GPIO/ Bank 5 VREF
274	AF7	BK5_IO_N18/VRP	T.B.D.	GPIO/ Bank 5 VRP
275	W12	BK5_IO_P6	T.B.D.	GPIO
276	AE8	BK5_IO_P15	T.B.D.	GPIO
277	AA11	BK5_IO_P8	T.B.D.	GPIO
278	AF8	BK5_IO_N15	T.B.D.	GPIO
279	AB11	BK5_IO_N8	T.B.D.	GPIO
280	AE10	BK5_IO_P10*	T.B.D.	GPIO
281	AA13	BK5_IO_S2	T.B.D.	GPIO
282	AF10	BK5_IO_N10*	T.B.D.	GPIO
283	AD13	BK5_IO_P1/CLK2	T.B.D.	GPIO/GCLK
284	AE11	BK5_IO_P7*	T.B.D.	GPIO/GCLK
285	AE13	BK5_IO_N1/CLK3	T.B.D.	GPIO
286	AF11	BK5_IO_N7*	T.B.D.	GPIO
287	Y13	BK5_IO_N3	T.B.D.	GPIO
288	AE12	BK5_IO_P4/VREF	T.B.D.	GPIO/ Bank 5 VREF
289	W13	BK5_IO_P3	T.B.D.	GPIO
290	AF12	BK5_IO_N4	T.B.D.	GPIO
291	AD15	BK4_IO_S2	T.B.D.	GPIO
292	AF13	BK5_IO_S1/VREF	T.B.D.	GPIO/ Bank 5 VREF
293	AE15	BK4_IO_N4	T.B.D.	GPIO
294	AE14	BK4_IO_N1/CLK1	T.B.D.	GPIO/GCLK
295	AF15	BK4_IO_P4	T.B.D.	GPIO
296	AF14	BK4_IO_P1/CLK0	Clock signal from on board oscillator when populated	GPIO/GCLK
297	--	GND	Ground	
298	--	GND		
299	--	VCC_5	Power supply for FPGA IO bank 4 and bank 5	
300	--	VCC_5		
301	--	VCC_4		
302	--	VCC_4		
303	--	GND	Ground	
304	--	GND		
305	AB14	BK4_IO_S1/VREF	T.B.D.	GPIO/ Bank 4 VREF
306	AD19	BK4_IO_S6*	T.B.D.	GPIO
307	AE16	BK4_IO_N7*	T.B.D.	GPIO
308	AF20	BK4_IO_P19	T.B.D.	GPIO
309	AF16	BK4_IO_P7/VREF*	T.B.D.	GPIO/ Bank 4 VREF
310	AE20	BK4_IO_N19	T.B.D.	GPIO
311	AB18	BK4_IO_N14*	T.B.D.	GPIO
312	AF21	BK4_IO_S8	T.B.D.	GPIO
313	AC18	BK4_IO_P14*	T.B.D.	GPIO
314	AF22	BK4_IO_S9	T.B.D.	GPIO
315	AE19	BK4_IO_N16	T.B.D.	GPIO
316	AB16	BK4_IO_N8	T.B.D.	GPIO
317	AF19	BK4_IO_P16	T.B.D.	GPIO
318	AC16	BK4_IO_P8	T.B.D.	GPIO
319	AB15	BK4_IO_P5	T.B.D.	GPIO
320	AD17	BK4_IO_N11/VREF	T.B.D.	GPIO/ Bank 4 VREF
321	AA15	BK4_IO_N5	T.B.D.	GPIO
322	AB17	BK4_IO_P11	T.B.D.	GPIO
323	Y16	BK4_IO_N9	T.B.D.	GPIO

Connector JB3	FPGA		Description	
Pin	Pin	Name	System	FPGA module
324	AF17	BK4_IO_P10*	T.B.D.	GPIO
325	AA16	BK4_IO_P9	T.B.D.	GPIO
326	AE17	BK4_IO_N10*	T.B.D.	GPIO
327	AC17	BK4_IO_N12	T.B.D.	GPIO
328	W15	BK4_IO_S3	T.B.D.	GPIO
329	AA17	BK4_IO_P12	T.B.D.	GPIO
330	W16	BK4_IO_S4	T.B.D.	GPIO
331	Y17	BK4_IO_S5/VREF	T.B.D.	GPIO/ Bank 4 VREF
332	AE18	BK4_IO_P13*	T.B.D.	GPIO
333	AA18	BK4_IO_P15	T.B.D.	GPIO
334	AD18	BK4_IO_N13*	T.B.D.	GPIO
335	Y18	BK4_IO_N15	T.B.D.	GPIO
336	AB19	BK4_IO_N17*	T.B.D.	GPIO
337	AA19	BK4_IO_P18*	T.B.D.	GPIO
338	AC19	BK4_IO_P17*	T.B.D.	GPIO
339	Y19	BK4_IO_N18*	T.B.D.	GPIO
340	AC20	BK4_IO_P20	T.B.D.	GPIO
341	AA20	BK4_IO_S7	T.B.D.	GPIO
342	AB20	BK4_IO_N20	T.B.D.	GPIO
343	AC21	BK4_IO_P22	T.B.D.	GPIO
344	AE21	BK4_IO_P21	T.B.D.	GPIO
345	AB21	BK4_IO_N22	T.B.D.	GPIO
346	AD21	BK4_IO_N21	T.B.D.	GPIO
347	AE22	BK4_IO_P23	T.B.D.	GPIO
348	AE23	BK4_IO_N24	T.B.D.	GPIO
349	AD22	BK4_IO_N23/VREF	T.B.D.	GPIO/ Bank 4 VREF
350	AF23	BK4_IO_P24	T.B.D.	GPIO
351	AC22	BK4_IO_P26/VRN	T.B.D.	GPIO/ Bank 4 VRN
352	AE24	BK4_IO_N25	T.B.D.	GPIO
353	AB22	BK4_IO_N26/VRP	T.B.D.	GPIO/ Bank 4 VRP
354	AF24	BK4_IO_P25	T.B.D.	GPIO
355	AD25	BK4_IO_S11/VREF	T.B.D.	GPIO/ Bank 4 VREF
356	AD23	BK4_IO_S10	T.B.D.	GPIO
357	--	GND	Ground	
358	--	GND		
359	--	+3.3v	+3.3v power supply	
360	--	+3.3v		

Connector JB4	FPGA		Description	
Pin	Pin	Name	System	FPGA module
361	--	+3.3v	+3.3v power supply	
362	--	+3.3v		
363	--	GND	Ground	
364	--	GND		
365	--	NC	Not connected	
366	--	NC	Not connected	
367	--	NC	Not connected	
368	--	NC	Not connected	
369	--	NC	Not connected	
370	--	NC	Not connected	
371	--	NC	Not connected	
372	--	NC	Not connected	
373	--	NC	Not connected	
374	--	NC	Not connected	
375	--	NC	Not connected	
376	--	NC	Not connected	
377	--	NC	Not connected	
378	--	NC	Not connected	
379	--	NC	Not connected	
380	--	NC	Not connected	
381	R2	BK6_IO_N5/VREF	T.B.D.	GPIO/ Bank 6 VREF
382	--	NC	Not connected	
383	R1	BK6_IO_P5	T.B.D.	GPIO
384	--	NC	Not connected	
385	T1	BK6_IO_P9	T.B.D.	GPIO
386	P8	BK6_IO_N4	T.B.D.	GPIO

Connector JB4	FPGA		Description	
Pin	Pin	Name	System	FPGA module
387	T2	BK6_IO_N9	T.B.D.	GPIO
388	P7	BK6_IO_P4	T.B.D.	GPIO
389	P6	BK6_IO_N3	T.B.D.	GPIO
390	T8	BK6_IO_N11	T.B.D.	GPIO
391	P5	BK6_IO_P3	T.B.D.	GPIO
392	T7	BK6_IO_P11	T.B.D.	GPIO
393	U3	BK6_IO_P13	T.B.D.	GPIO
394	T6	BK6_IO_N10	T.B.D.	GPIO
395	U4	BK6_IO_N13/VREF	T.B.D.	GPIO/ Bank 6 VREF
396	T5	BK6_IO_P10	T.B.D.	GPIO
397	P1	BK6_IO_P1/VREF	T.B.D.	GPIO/ Bank 6 VREF
398	R6	BK6_IO_N7	T.B.D.	GPIO
399	P2	BK6_IO_N1	T.B.D.	GPIO
400	R5	BK6_IO_P7	T.B.D.	GPIO
401	U7	BK6_IO_P17	T.B.D.	GPIO
402	R8	BK6_IO_N8	T.B.D.	GPIO
403	V7	BK6_IO_N17	T.B.D.	GPIO
404	R7	BK6_IO_P8	T.B.D.	GPIO
405	V6	BK6_IO_N20	T.B.D.	GPIO
406	U5	BK6_IO_P14	T.B.D.	GPIO
407	W5	BK6_IO_P20	T.B.D.	GPIO
408	U6	BK6_IO_N14	T.B.D.	GPIO
409	W6	BK6_IO_P21	T.B.D.	GPIO
410	R3	BK6_IO_P6	T.B.D.	GPIO
411	W7	BK6_IO_N21	T.B.D.	GPIO
412	T4	BK6_IO_N6	T.B.D.	GPIO
413	Y6	BK6_IO_P26*	T.B.D.	GPIO
414	P3	BK6_IO_P2	T.B.D.	GPIO
415	Y7	BK6_IO_N26*	T.B.D.	GPIO
416	P4	BK6_IO_N2	T.B.D.	GPIO
417	--	GND	Ground	
418	--	GND		
419	--	VCC_7	Power supply for FPGA IO bank 7 can be taken from internal 2.5V, internal 3.3V, external JB4 or external JT1.	
420	--	VCC_7		
421	--	VCC_6	Power supply for FPGA IO bank 6.	
422	--	VCC_6		
423	--	GND	Ground	
424	--	GND		
425	--	GND		
426	U2	BK6_IO_N12	T.B.D.	GPIO
427	V5	BK6_IO_N16	T.B.D.	GPIO
428	U1	BK6_IO_P12	T.B.D.	GPIO
429	V4	BK6_IO_P16	T.B.D.	GPIO
430	V3	BK6_IO_N15	T.B.D.	GPIO
431	W4	BK6_IO_N19	T.B.D.	GPIO
432	V2	BK6_IO_P15	T.B.D.	GPIO
433	W3	BK6_IO_P19/VREF	T.B.D.	GPIO/ Bank 6 VREF
434	W1	BK6_IO_P18	T.B.D.	GPIO
435	Y1	BK6_IO_P22*	T.B.D.	GPIO
436	W2	BK6_IO_N18	T.B.D.	GPIO
437	Y2	BK6_IO_N22*	T.B.D.	GPIO
438	Y4	BK6_IO_P24*	T.B.D.	GPIO
439	AA4	BK6_IO_N25*	T.B.D.	GPIO
440	Y5	BK6_IO_N24*	T.B.D.	GPIO
441	AA3	BK6_IO_P25*	T.B.D.	GPIO
442	AA1	BK6_IO_P23*	T.B.D.	GPIO
443	**AA5**	**BK6_IO_S1*** **	**Not present in XC3S1500**	**GPIO**
444	AA2	BK6_IO_N23/VREF*	T.B.D.	GPIO/ Bank 6 VREF
445	AB3	BK6_IO_P29	T.B.D.	GPIO
446	AB1	BK6_IO_P27*	T.B.D.	GPIO
447	AB4	BK6_IO_N29	T.B.D.	GPIO
448	AB2	BK6_IO_N27*	T.B.D.	GPIO
449	AB6	BK5_IO_N23	T.B.D.	GPIO
450	AC1	BK6_IO_P28	T.B.D.	GPIO
451	AA6	BK5_IO_P23	T.B.D.	GPIO
452	AC2	BK6_IO_N28/VREF	T.B.D.	GPIO/ Bank 6 VREF
453	AA7	BK5_IO_S9	T.B.D.	GPIO
454	AD1	BK6_IO_P30/VRN	T.B.D.	GPIO/ Bank 6 VRN
455	AD4	BK5_IO_P24	T.B.D.	GPIO

Connector JB4	FPGA		Description	
Pin	Pin	Name	System	FPGA module
456	AD2	BK6_IO_N30/VRP	T.B.D.	GPIO/ Bank 6 VRP
457	AE4	BK5_IO_N24	T.B.D.	GPIO
458	AA8	BK5_IO_P17*	T.B.D.	GPIO
459	AD5	BK5_IO_P22	T.B.D.	GPIO
460	AB8	BK5_IO_N17/VREF*	T.B.D.	GPIO/ Bank 6 VREF
461	AE5	BK5_IO_N22	T.B.D.	GPIO
462	Y8	BK5_IO_S8	T.B.D.	GPIO
463	AB7	BK5_IO_P19	T.B.D.	GPIO
464	AC9	BK5_IO_S6*	T.B.D.	GPIO
465	AC7	BK5_IO_N19	T.B.D.	GPIO
466	Y10	BK5_IO_P12/VREF	T.B.D.	GPIO/ Bank 6 VREF
467	AD8	BK5_IO_N16*	T.B.D.	GPIO
468	AA10	BK5_IO_N12	T.B.D.	GPIO
469	AC8	BK5_IO_P16*	T.B.D.	GPIO
470	AA9	BK5_IO_N14	T.B.D.	GPIO
471	AD9	BK5_IO_P13*	T.B.D.	GPIO
472	Y9	BK5_IO_P14	T.B.D.	GPIO
473	AE9	BK5_IO_N13*	T.B.D.	GPIO
474	AC6	BK5_IO_P21	T.B.D.	GPIO
475	AB9	BK5_IO_S7	T.B.D.	GPIO
476	AD6	BK5_IO_N21	T.B.D.	GPIO
477	--	GND	Ground	
478	--	GND		
479	--	+3.3v	+3.3v power supply	
480	--	+3.3v		

2.2 Top connectors

The connectors JT1 and JT2 located on the top layer are high speed SAMTEC QSH-060-02-L-D-A connectors that mate to SAMTEC QTH-060-02-L-D-A connectors.

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
1	--	+3.3v	+3.3v power supply	
2	--	+3.3v		
3	--	GND	Ground	
4	--	GND		
5	F5	BK7_IO_N30/VRP	T.B.D.	GPIO/Bank 7 VRP
6	H5	BK7_IO_P20/VREF	T.B.D.	GPIO/Bank 7 VREF
7	F6	BK7_IO_P30/VRN	T.B.D.	GPIO/Bank 7 VRN
8	J6	BK7_IO_N20	T.B.D.	GPIO
9	G6	BK7_IO_N27*	T.B.D.	GPIO
10	J5	BK7_IO_P16	T.B.D.	GPIO
11	G7	BK7_IO_P27*	T.B.D.	GPIO
12	J4	BK7_IO_N16	T.B.D.	GPIO
13	H6	BK7_IO_N22*	T.B.D.	GPIO
14	M7	BK7_IO_N8	T.B.D.	GPIO
15	H7	BK7_IO_P22/VREF*	T.B.D.	GPIO/Bank 7 VREF
16	M8	BK7_IO_P8	T.B.D.	GPIO
17	N5	BK7_IO_N3	T.B.D.	GPIO
18	M6	BK7_IO_N7	T.B.D.	GPIO
19	N6	BK7_IO_P3	T.B.D.	GPIO
20	M5	BK7_IO_P7	T.B.D.	GPIO
21	F4	BK7_IO_P25*	T.B.D.	GPIO
22	D2	BK7_IO_P28	T.B.D.	GPIO
23	F3	BK7_IO_N25*	T.B.D.	GPIO
24	D1	BK7_IO_N28/VREF	T.B.D.	GPIO/Bank 7 VREF
25	G5	BK7_IO_P24*	T.B.D.	GPIO
26	E2	BK7_IO_P26*	T.B.D.	GPIO
27	G4	BK7_IO_N24*	T.B.D.	GPIO
28	E1	BK7_IO_N26*	T.B.D.	GPIO
29	L4	BK7_IO_P6	T.B.D.	GPIO

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
30	F2	BK7_IO_P23*	T.B.D.	GPIO
31	M3	BK7_IO_N6	T.B.D.	GPIO
32	F1	BK7_IO_N23*	T.B.D.	GPIO
33	H3	BK7_IO_N19	T.B.D.	GPIO
34	G2	BK7_IO_P21	T.B.D.	GPIO
35	H4	BK7_IO_P19	T.B.D.	GPIO
36	G1	BK7_IO_N21	T.B.D.	GPIO
37	J3	BK7_IO_P15	T.B.D.	GPIO
38	H2	BK7_IO_P18	T.B.D.	GPIO
39	J2	BK7_IO_N15	T.B.D.	GPIO
40	H1	BK7_IO_N18/VREF	T.B.D.	GPIO/Bank 7 VREF
41	J7	BK7_IO_P17	T.B.D.	GPIO
42	K2	BK7_IO_P12	T.B.D.	GPIO
43	C14	BK1_IO_P1/CLK4	T.B.D.	GPIO
44	K1	BK7_IO_N12	T.B.D.	GPIO/GCLK
45	B14	BK1_IO_N1/CLK5	T.B.D.	GPIO
46	L2	BK7_IO_P9	T.B.D.	GPIO/GCLK
47	K3	BK7_IO_N13	T.B.D.	GPIO
48	L1	BK7_IO_N9	T.B.D.	GPIO
49	K4	BK7_IO_P13	T.B.D.	GPIO
50	M2	BK7_IO_P5	T.B.D.	GPIO
51	K7	BK7_IO_N17	T.B.D.	GPIO
52	M1	BK7_IO_N5	T.B.D.	GPIO
53	L5	BK7_IO_N10	T.B.D.	GPIO
54	N2	BK7_IO_P1	T.B.D.	GPIO
55	L6	BK7_IO_P10	T.B.D.	GPIO
56	N1	BK7_IO_N1/VREF	T.B.D.	GPIO/Bank 7 VREF
57	--	GND	Ground	
58	--	GND		
59	--	VCC_7	Power supply for FPGA IO bank 7 can be taken from internal 2.5V, internal 3.3V, external JB4 or external JT1.	
60	--	VCC_7		
61	--	VCC_7		
62	--	VCC_7		
63	--	GND	Ground	
64	--	GND		
65	K6	BK7_IO_P14	T.B.D.	GPIO
66	N7	BK7_IO_N4	T.B.D.	GPIO
67	K5	BK7_IO_N14	T.B.D.	GPIO
68	N8	BK7_IO_P4	T.B.D.	GPIO
69	E4	BK7_IO_P29	T.B.D.	GPIO
70	L8	BK7_IO_P11/VREF	T.B.D.	GPIO/Bank 7 VREF
71	E3	BK7_IO_N29	T.B.D.	GPIO
72	L7	BK7_IO_N11	T.B.D.	GPIO
73	N3	BK7_IO_N2	T.B.D.	GPIO
74	--	NC	Not connected	
75	N4	BK7_IO_P2	T.B.D.	GPIO
76	--	NC	Not connected	
77	--	NC	Not connected	
78	--	NC	Not connected	
79	--	NC	Not connected	
80	--	NC	Not connected	
81	--	NC	Not connected	
82	--	NC	Not connected	
83	--	NC	Not connected	
84	--	NC	Not connected	
85	--	NC	Not connected	
86	--	NC	Not connected	
87	--	NC	Not connected	
88	--	NC	Not connected	
89	--	NC	Not connected	
90	--	NC	Not connected	
91	--	NC	Not connected	
92	--	NC	Not connected	
93	--	NC	Not connected	
94	--	NC	Not connected	
95	--	NC	Not connected	
96	--	NC	Not connected	
97	--	NC	Not connected	
98	--	NC	Not connected	

Connector JT1	FPGA		Description	
Pin	Pin	Name	System	FPGA module
99	--	NC	Not connected	
100	--	NC	Not connected	
101	--	NC	Not connected	
102	--	NC	Not connected	
103	--	NC	Not connected	
104	--	NC	Not connected	
105	--	NC	Not connected	
106	--	NC	Not connected	
107	--	NC	Not connected	
108	--	NC	Not connected	
109	--	NC	Not connected	
110	--	NC	Not connected	
111	--	NC	Not connected	
112	--	NC	Not connected	
113	AF4	BK5_IO_S11	T.B.D.	GPIO
114	--	NC	Not connected	
115	AD12	BK5_IO_S3	T.B.D.	GPIO
116	--	NC	Not connected	
117	--	GND	Ground	
118	--	GND		
119	--	+3.3v	+3.3v power supply	
120	--	+3.3v		

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
121	--	+3.3v	+3.3v power supply	
122	--	+3.3v		
123	--	GND	Ground	
124	--	GND		
125	--	NC	Not Connected	
126	--	NC	Not Connected	
127	--	NC	Not Connected	
128	--	NC	Not Connected	
129	--	NC	Not Connected	
130	--	NC	Not Connected	
131	--	NC	Not Connected	
132	--	NC	Not Connected	
133	--	NC	Not Connected	
134	--	NC	Not Connected	
135	--	NC	Not Connected	
136	--	NC	Not Connected	
137	--	NC	Not Connected	
138	--	NC	Not Connected	
139	--	NC	Not Connected	
140	--	NC	Not Connected	
141	--	NC	Not Connected	
142	--	NC	Not Connected	
143	--	NC	Not Connected	
144	--	NC	Not Connected	
145	--	NC	Not Connected	
146	--	NC	Not Connected	
147	--	NC	Not Connected	
148	--	NC	Not Connected	
149	--	NC	Not Connected	
150	--	NC	Not Connected	
151	--	NC	Not Connected	
152	--	NC	Not Connected	
153	--	NC	Not Connected	
154	--	NC	Not Connected	
155	--	NC	Not Connected	
156	--	NC	Not Connected	
157	--	NC	Not Connected	
158	--	NC	Not Connected	
159	--	NC	Not Connected	
160	--	NC	Not Connected	
161	--	NC	Not Connected	
162	P23	BK3_IO_P2	T.B.D.	GPIO

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
163	--	NC	Not Connected	
164	P24	BK3_IO_N2	T.B.D.	GPIO
165	--	NC	Not Connected	
166	T21	BK3_IO_P10	T.B.D.	GPIO
167	R19	BK3_IO_P8	T.B.D.	GPIO
168	T22	BK3_IO_N10	T.B.D.	GPIO
169	R20	BK3_IO_N8	T.B.D.	GPIO
170	W24	BK3_IO_N19	T.B.D.	GPIO
171	T19	BK3_IO_P11	T.B.D.	GPIO
172	Y23	BK3_IO_N24*	T.B.D.	GPIO
173	T20	BK3_IO_N11	T.B.D.	GPIO
174	Y22	BK3_IO_P24*	T.B.D.	GPIO
175	P19	BK3_IO_P4	T.B.D.	GPIO
176	AA24	BK3_IO_N25*	T.B.D.	GPIO
177	--	GND	Ground	
178	--	GND		
179	--	VCC_3	Power supply for FPGA IO bank 3 can be taken from internal 2.5V, internal 3.3V, external JB2 or external JT2.	
180	--	VCC_3		
181	--	VCC_3		
182	--	VCC_3		
183	--	GND	Ground	
184	--	GND		
185	P20	BK3_IO_N4	T.B.D.	GPIO
186	P21	BK3_IO_P3	T.B.D.	GPIO
187	P25	BK3_IO_P1	T.B.D.	GPIO
188	P22	BK3_IO_N3	T.B.D.	GPIO
189	P26	BK3_IO_N1/VREF	T.B.D.	GPIO/Bank 3 VREF
190	R22	BK3_IO_N7	T.B.D.	GPIO
191	R25	BK3_IO_P5/VREF	T.B.D.	GPIO/Bank 3 VREF
192	R21	BK3_IO_P7	T.B.D.	GPIO
193	R26	BK3_IO_N5	T.B.D.	GPIO
194	R24	BK3_IO_N6	T.B.D.	GPIO
195	T25	BK3_IO_P9	T.B.D.	GPIO
196	T23	BK3_IO_P6	T.B.D.	GPIO
197	T26	BK3_IO_N9	T.B.D.	GPIO
198	U22	BK3_IO_N14	T.B.D.	GPIO
199	U25	BK3_IO_P12	T.B.D.	GPIO
200	U21	BK3_IO_P14/VREF	T.B.D.	GPIO/Bank 3 VREF
201	U26	BK3_IO_N12	T.B.D.	GPIO
202	U20	BK3_IO_N17	T.B.D.	GPIO
203	V25	BK3_IO_N15	T.B.D.	GPIO
204	V20	BK3_IO_P17	T.B.D.	GPIO
205	V24	BK3_IO_P15	T.B.D.	GPIO
206	V21	BK3_IO_N20	T.B.D.	GPIO
207	W26	BK3_IO_N18	T.B.D.	GPIO
208	W22	BK3_IO_P20	T.B.D.	GPIO
209	W25	BK3_IO_P18	T.B.D.	GPIO
210	W21	BK3_IO_N22*	T.B.D.	GPIO
211	Y26	BK3_IO_N21	T.B.D.	GPIO
212	W20	BK3_IO_P22*	T.B.D.	GPIO
213	Y25	BK3_IO_P21	T.B.D.	GPIO
214	Y21	BK3_IO_N27*	T.B.D.	GPIO
215	AA26	BK3_IO_N23*	T.B.D.	GPIO
216	Y20	BK3_IO_P27*	T.B.D.	GPIO
217	AA25	BK3_IO_P23/VREF*	T.B.D.	GPIO/Bank 3 VREF
218	AA22	BK3_IO_N30/VRP	T.B.D.	GPIO/Bank 3 VRP
219	AB26	BK3_IO_N26*	T.B.D.	GPIO
220	AA21	BK3_IO_P30/VRN	T.B.D.	GPIO/Bank 3 VRN
221	AB25	BK3_IO_P26*	T.B.D.	GPIO
222	AA23	BK3_IO_P25*	T.B.D.	GPIO
223	AC26	BK3_IO_N28	T.B.D.	GPIO
224	AB24	BK3_IO_N29/VREF	T.B.D.	GPIO/Bank 3 VREF
225	AC25	BK3_IO_P28	T.B.D.	GPIO
226	AB23	BK3_IO_P29	T.B.D.	GPIO
227	U24	BK3_IO_N13	T.B.D.	GPIO
228	--	GND	Ground	
229	U23	BK3_IO_P13		GPIO
230	--	TDI_U	JTAG input data of upper board	
231	V22	BK3_IO_P16		GPIO

Connector JT2	FPGA		Description	
Pin	Pin	Name	System	FPGA module
232	--	TDO_U	JTAG output data of upper board	
233	V23	BK3_IO_N16	T.B.D.	GPIO
234	--	TMS	JTAG select signals	
235	W23	BK3_IO_P19/VREF	T.B.D.	GPIO/Bank 3 VREF
236	--	TCK	JTAG clock signal	
237	--	GND	Ground	
238	--	GND		
239	--	+3.3v	+3.3v power supply	
240	--	+3.3v		

3 Physical dimensions and footprints

Next figure shows the corresponding footprint that should be used on a carrier board that hosts an ERIZOV0-XC3S1500 FPGA module. The footprint is composed by 4 SAMTEC connectors of the type QSH-060-02-L-D-A. For more details on the pads relative location refer to the SAMTEC connector datasheet in http://www.samtec.com.

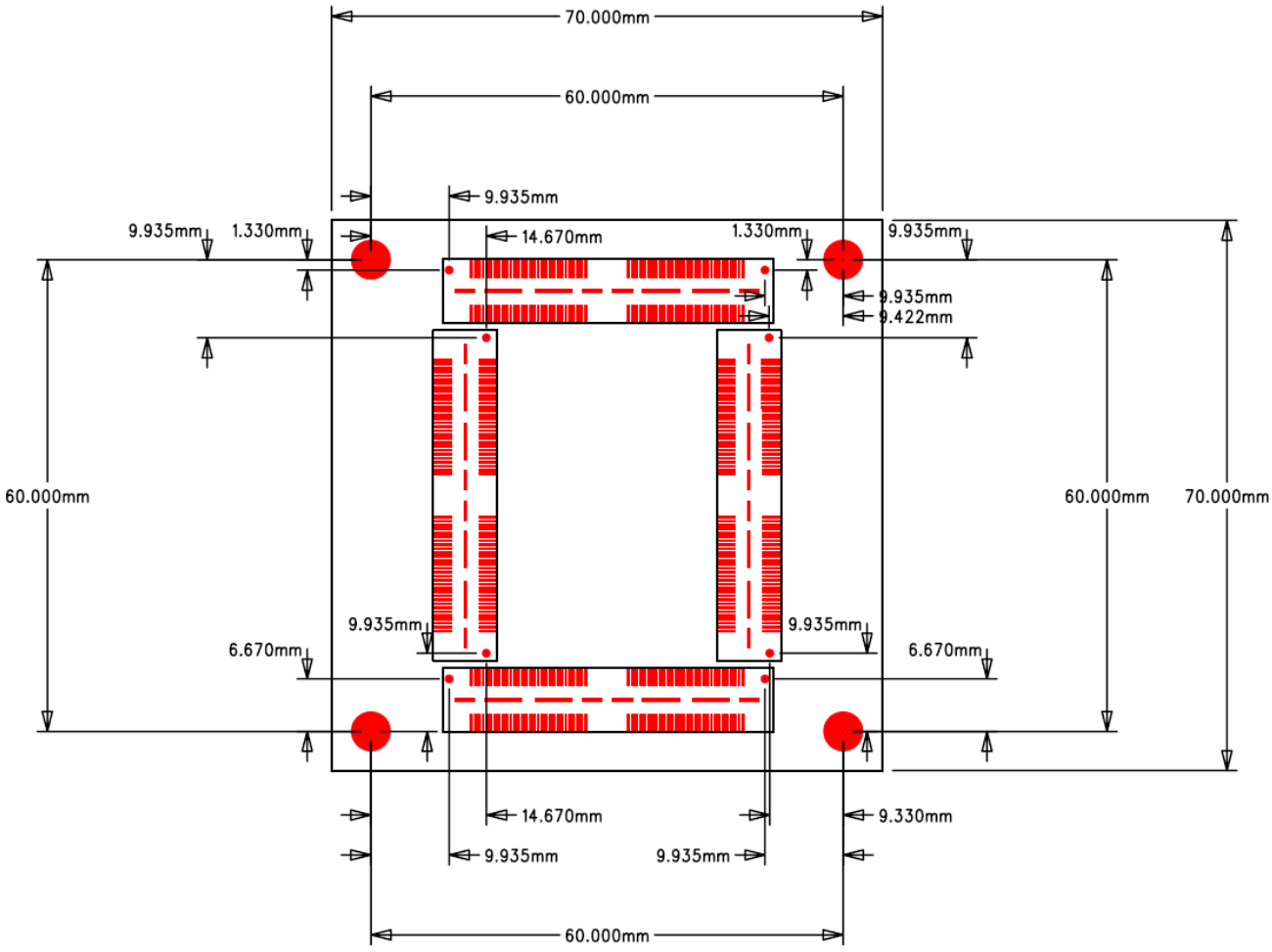


Figure 8. *ERIZOV0-XC3S1500 FPGA footprint for a carrier board*

Contact via email (info@ramdsp.com) for Power Logic schematics symbols and PADS layout software footprint libraries for ERIZOV0-XC2S1500 FPGA module.

Next figure shows the corresponding footprint that should be used on a satellite board that is connected on top of the ERIZOV0-XC3S1500 FPGA module. The footprint is composed by 2 SAMTEC connectors of the type QTH-060-02-L-D-A. For more details on the pads relative location refer to the SAMTEC connector datasheet in http://www.samtec.com.

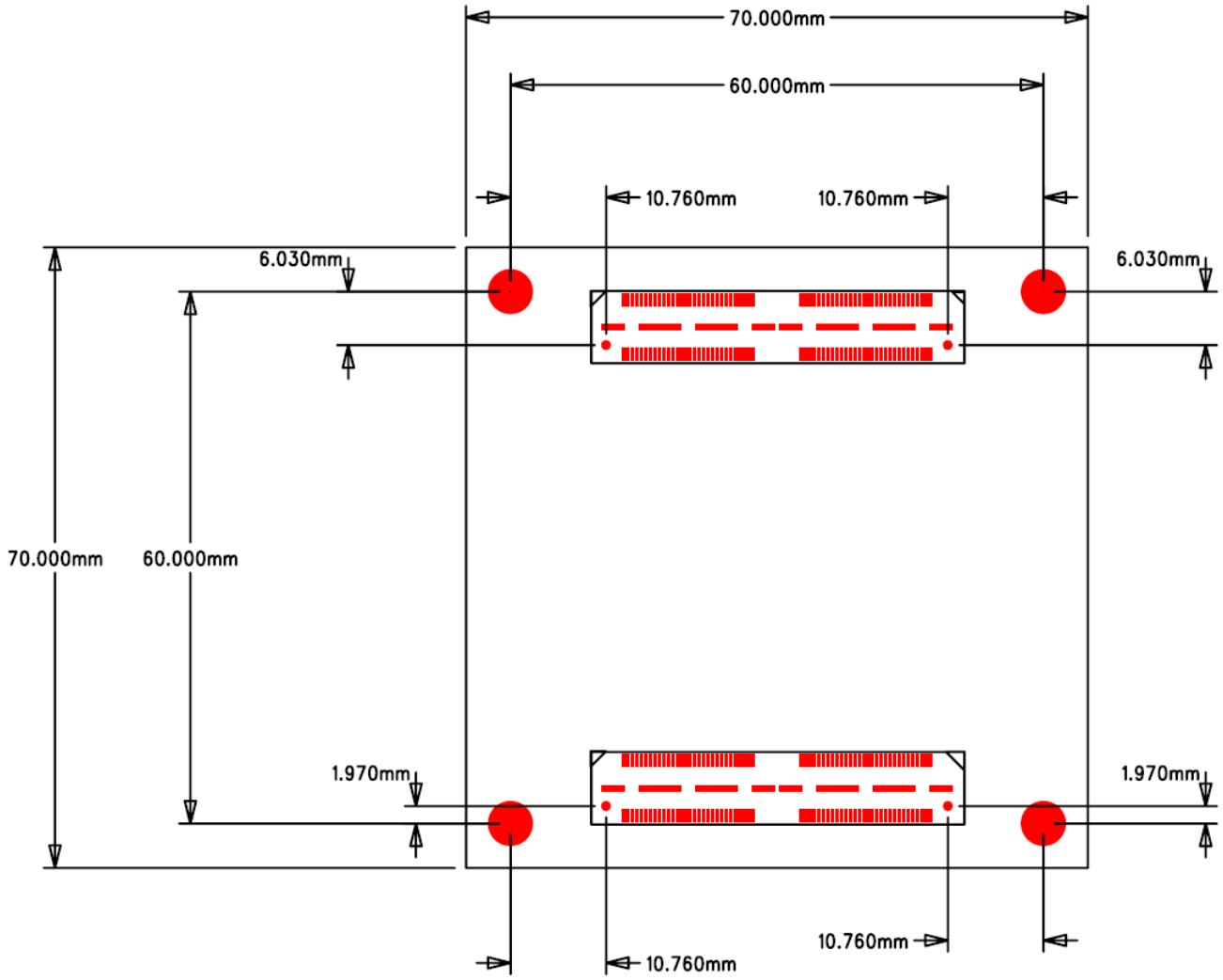


Figure 9. *ERIZOV0-XC3S1500 FPGA footprint for a satellite board*

Contact via email (info@ramdsp.com) for Power Logic schematics symbols and PADS layout software footprint libraries for ERIZOV0-XC2S1500 FPGA module.

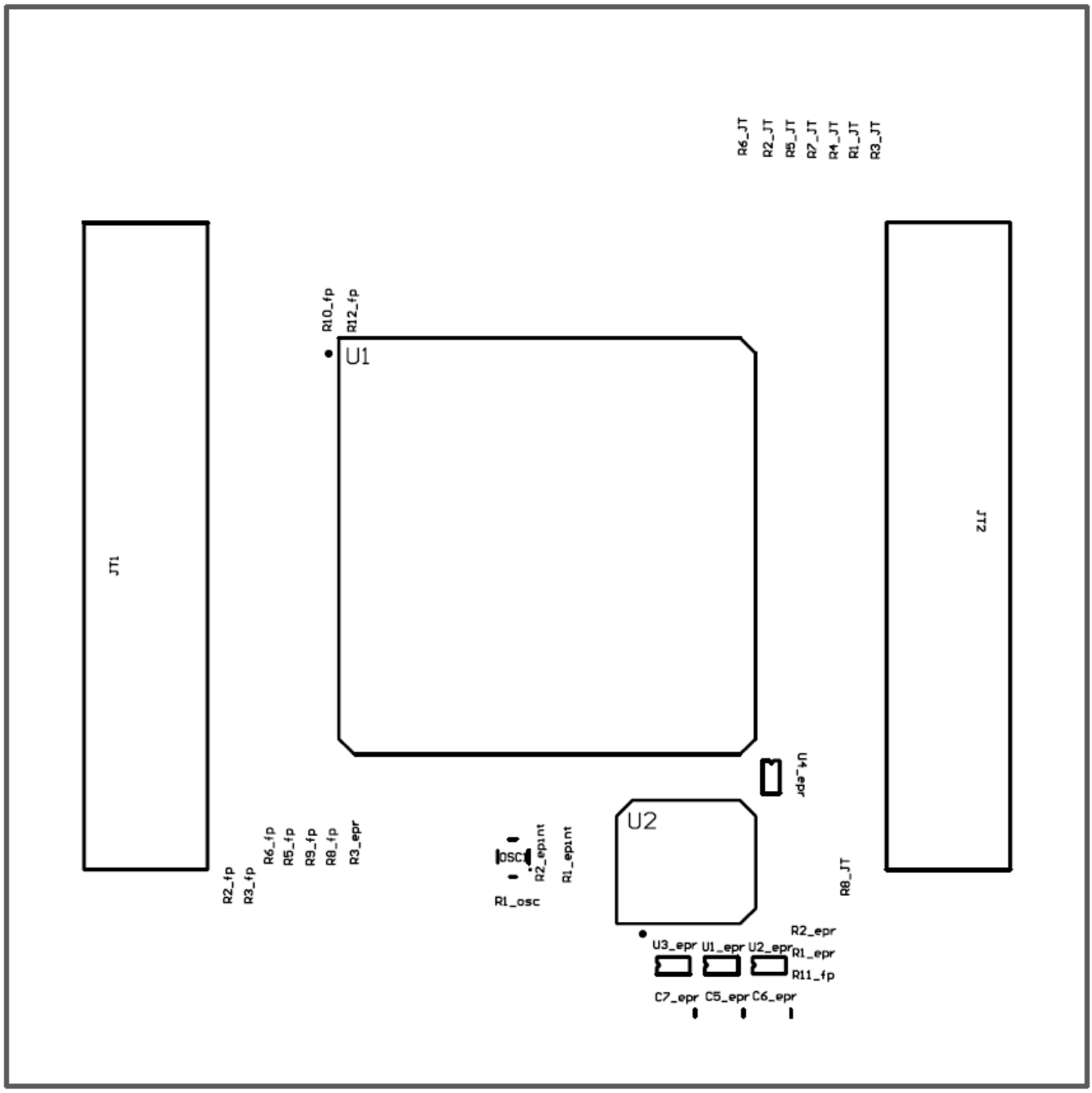


Figure 10. *ERIZOV0-XC3S1500 FPGA module top layer Silkscreen*

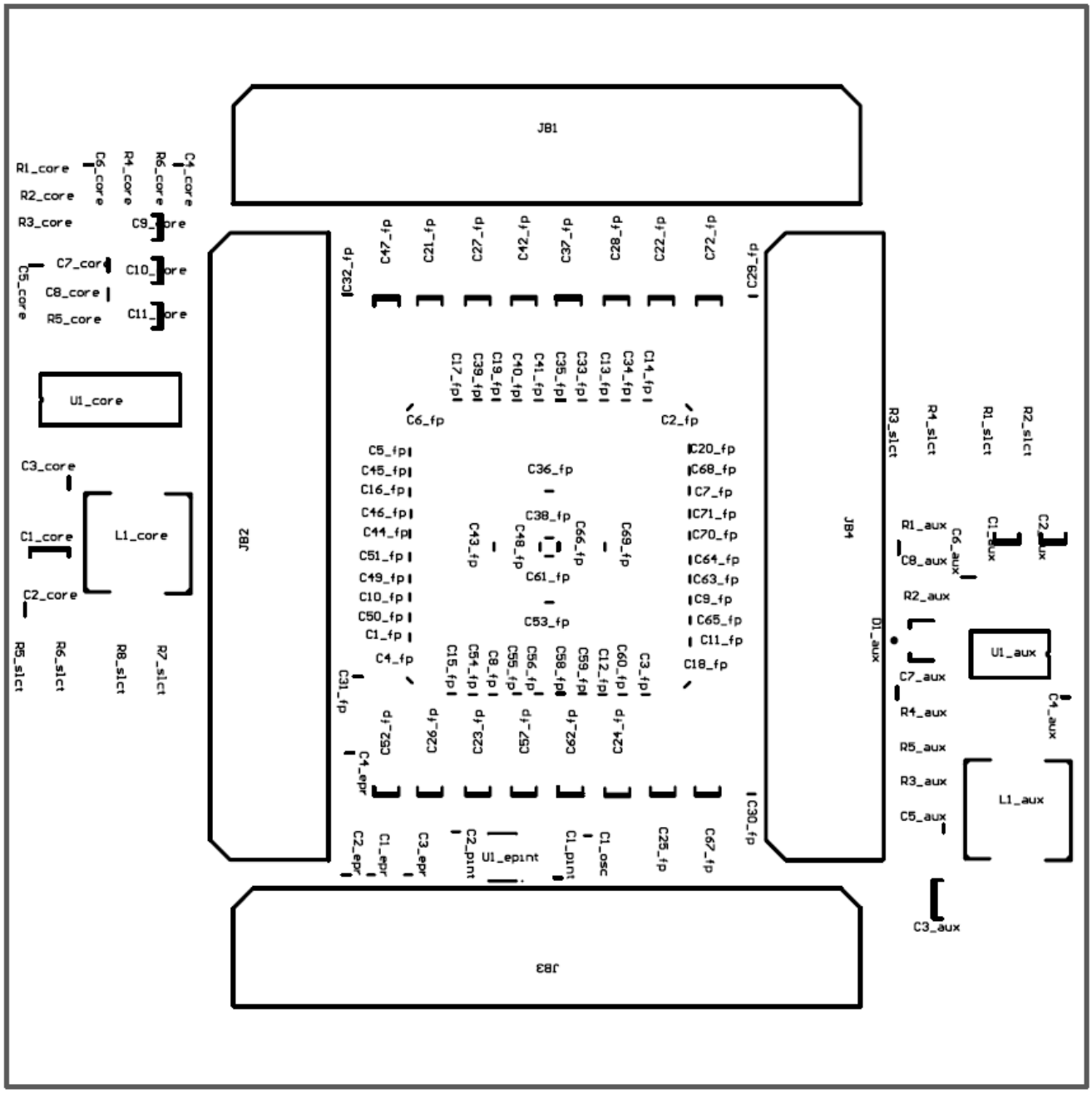


Figure 11. *ERIZOV0-XC3S1500 FPGA module bottom layer Silkscreen*

4 Accessories

The following devices are available for complementing the ERIZOV0-XC3S1500 FPGA module.

4.1 SDLCDv00 SDRAM module

The SDLCDv00 SDRAM module can be used on top of an ERIZOV0-XC3S1500 FPGA module and contains the following resources:

Qty.	Position	Resource	Description
1	U15	SODIMM 144	144 pin socket suitable for plugging a standard SDRAM SODIMM-144
1	U2	Flat cable connector	Flat cable connector for driving a Hitachi LCD module TX09D70VM1CCA.
1	U3	Touch screen controller	Philips UCB1400 touch screen controller and audio coder.
2	U1-A, U1-B	120 pin SAMTEC connector	Connectors compatible to FPGA module.

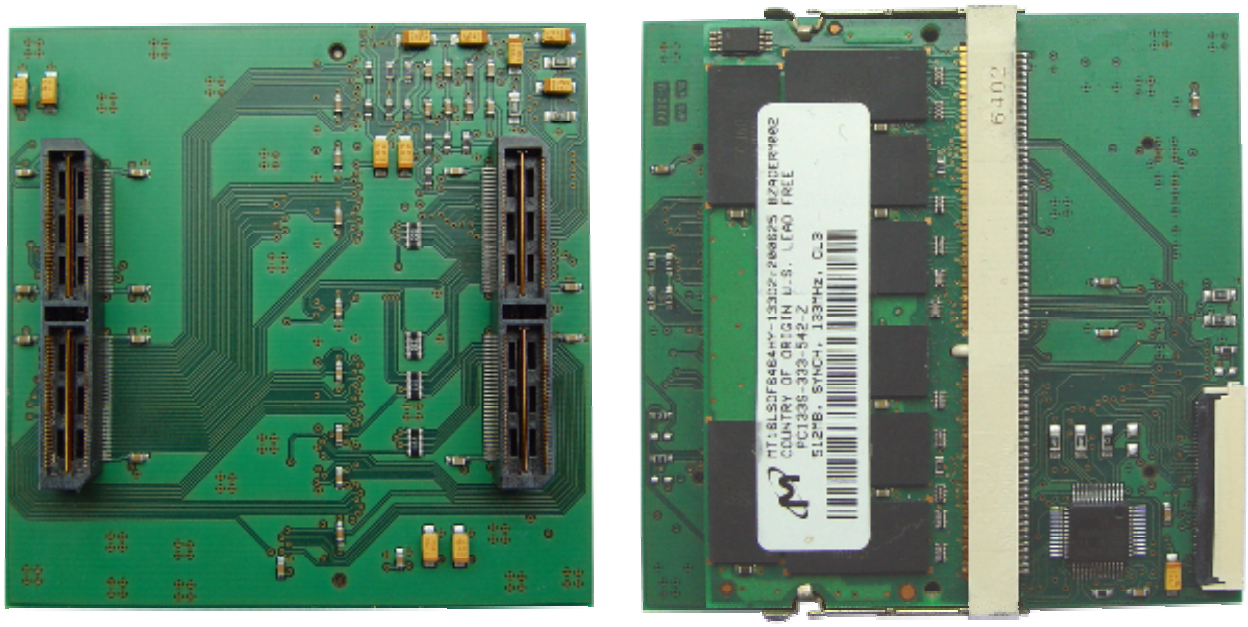


Figure 12. *SDLCDv00 SDRAM module bottom and top view*

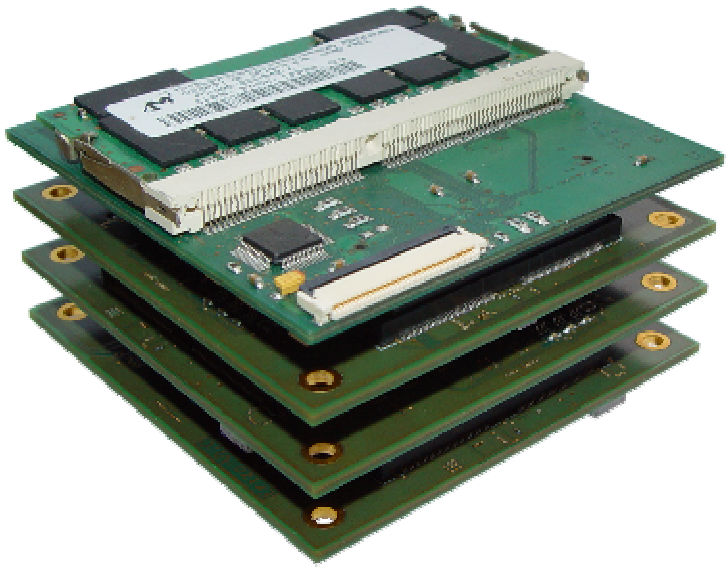


Figure 13. *SDLCDv00 SDRAM module application example*

Detailed information on SDLCDV00 module can be found in its corresponding hardware manual under http://www.ramdsp.com.

4.2 MESUDAQv00 Carrier Board

MESUDAQv00 carrier board gathers the hardware resources enumerated in the following table:

Qty.	Resource	Description
1	FPGA module	4 connectors suited for a single board FPGA module ERIZOV0-XC3S1500.
1	DSP module	2 connectors suited for a single board containing an Analog Devices Blackfin digital signal processor subsystem with the ADSP-BF537SKBC1600, 32MB of SDRAM, 4 MB of flash, and an Ethernet PHY unit.
1	SODIMM-144 socket	1 socket suited for a standard SDRAM module with up 512MB.
1	230V Power supply	20W AC-DC converter from 230V~ to +24V, and +/-15V. Protection circuit included.
1	3.3v power supply module.	Texas instruments TP6303N, 9,9W/3.3v DCDC switching voltage regulator supplying voltage to the digital parts of the system.
1	5v linear voltage regulator	MC78M05CDT linear voltage regulator generating 5v for analog components.
1	MMC socket	MMC socket whose control lines are connected to the DSP and FPGA modules.
2	Rotary encoder	User interface provided by rotary encoder. Connected to FPGA and DSP module.
1	CAN BUS port	CAN bus connection through a D-SUB9 male connector, can bus driver MCP2551 and can bus controller included in the Analog Devices BlackFin DSP.

2	RS232 port	RS232 serial connection through a D-SUB9 female connector. RS232 driver is the MAX3232 and the UART controllers are included in the Analog Devices BlackFin DSP. As an option, the UART lines can be controlled by the FPGA of the system.
1	Ethernet port	Ethernet connection through a RJ-45 connector The Ethernet controller and PHY module are included in the DSP module of the system.
2	Trigger input	Digital input accepting up to +/-24V. A BNC connector is available for every trigger input. After the BNC a MAX3232 driver is used to translate to 3.3v uni-polar signal level. The lines are connected to the FPGA of the system.
2	Active output	Digital output with +/-5V output range. A BNC connector is available for every active output. Before the BNC a MAX3232 driver is used to translate from 3.3v uni-polar signal level to 5v bipolar signalling. The control lines are connected to the FPGA of the system.
4	Clock lines	Dedicated clock line using SMA connector. Two of the clock lines are connected to global clock buffers of the FPGA of the system.
1	Expansion connector J1	Connector compatible to the analog to digital converter demo boards from Analog devices. Alternatively, it can be used as expansion connector with 49 digital GPIO lines controlled by the FPGA of the system.
1	Expansion connector J2	Connector compatible to the analog to digital converter demo boards from Linear Technology. Alternatively, it can be used as expansion connector with 18 digital GPIO lines controlled by the FPGA of the system.
1	JTAG connector.	14 pin 2.54mm pitch connector row as JTAG interface. Pin assignment compatible to the ICEbear JTAG cable.
1	Reset button	1 push button connected to the reset input of the Analog devices DSP module.
1	Analog output A	A differential high current analog output, The signal is generated by the texas instruments 165MSPS 14bit digital to analog converter DAC904. The output drivers are the linear technology LT1206CR, the outputs can swing up to +/-10V and supply up to 1,2A.
1	Triple Analog output B	A Texas Instruments triple 10bit 80MSPS digital to analog converter can be used to drive a VESA standard monitor through a DSUB15 connector.

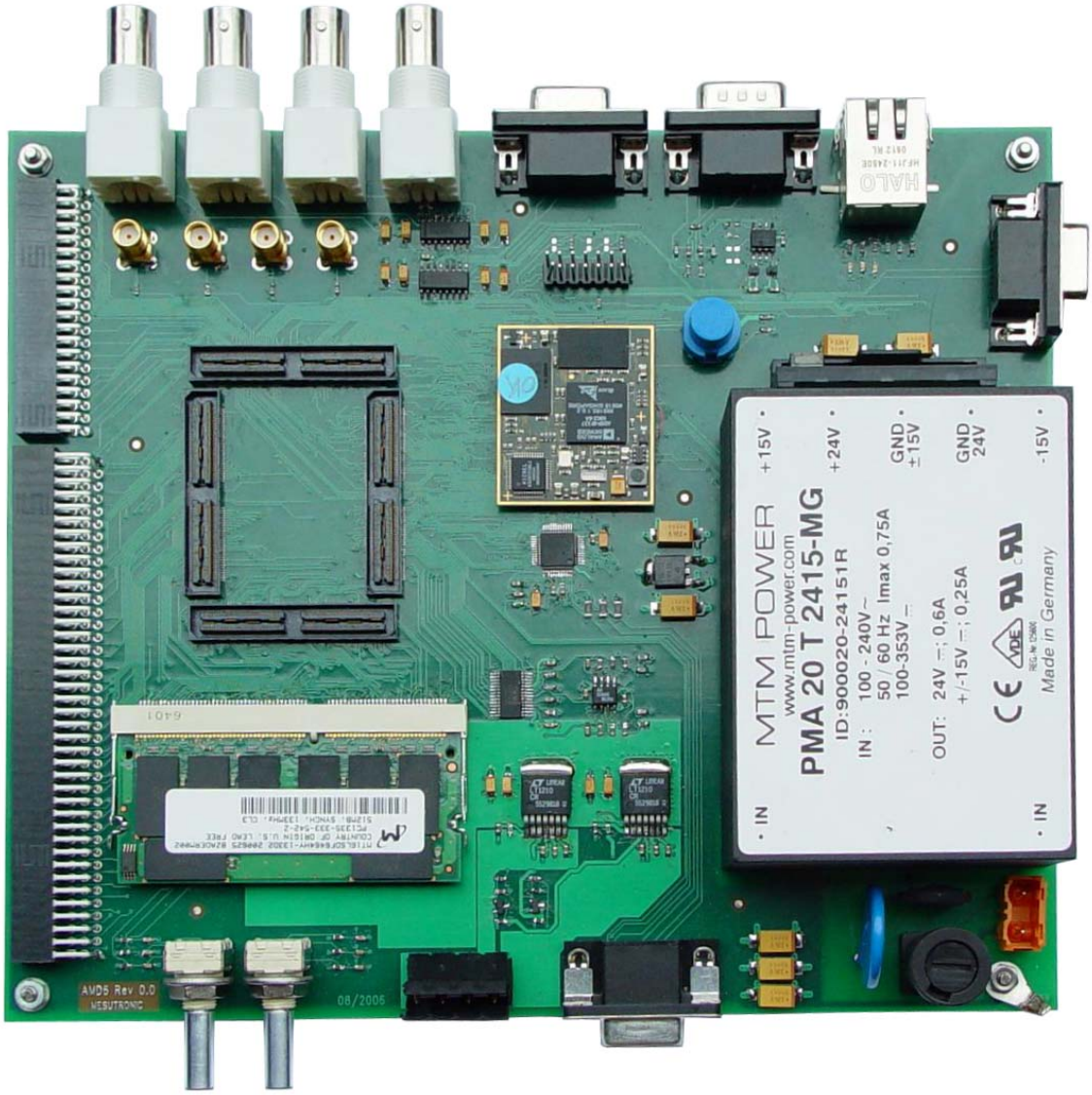


Figure 14. *MESUDAQv00 carrier board*

Detailed information on MESUDAQv00 carrier board can be found in its corresponding hardware manual under http://www.ramdsp.com.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